

Compal Confidential

Intel M/B Schematics Document

Kabylake-U(2+2)-DDR4 SODIMMx2 (1.2mm_6L)

~~nVidia N16 gDDR5-2GB~~

~~(N16S-6TR GM108-679/779 GeForce MX130)~~

~~(N16U-6MR1 GM108-625/725 GeForce MX110)~~

Date :2018-01-08

Version :v0.3

Project :20180PP_Harry Potter(15.6")

EPK50 :LA-G07DP

(EPK52 :LA-G07EP=>v0.2 for PV)

~~(EPK50 :KBLU_2G:LA-G07AP)~~

~~(EPK52 :KBLR_2G:LA-G07BP)~~

~~(EPK52 :KBLR_2G:LA-G07CP)~~

(EPK50 :KBLU:LA-G07DP)

(EPK52 :KBLR:LA-G07EP)

DIS

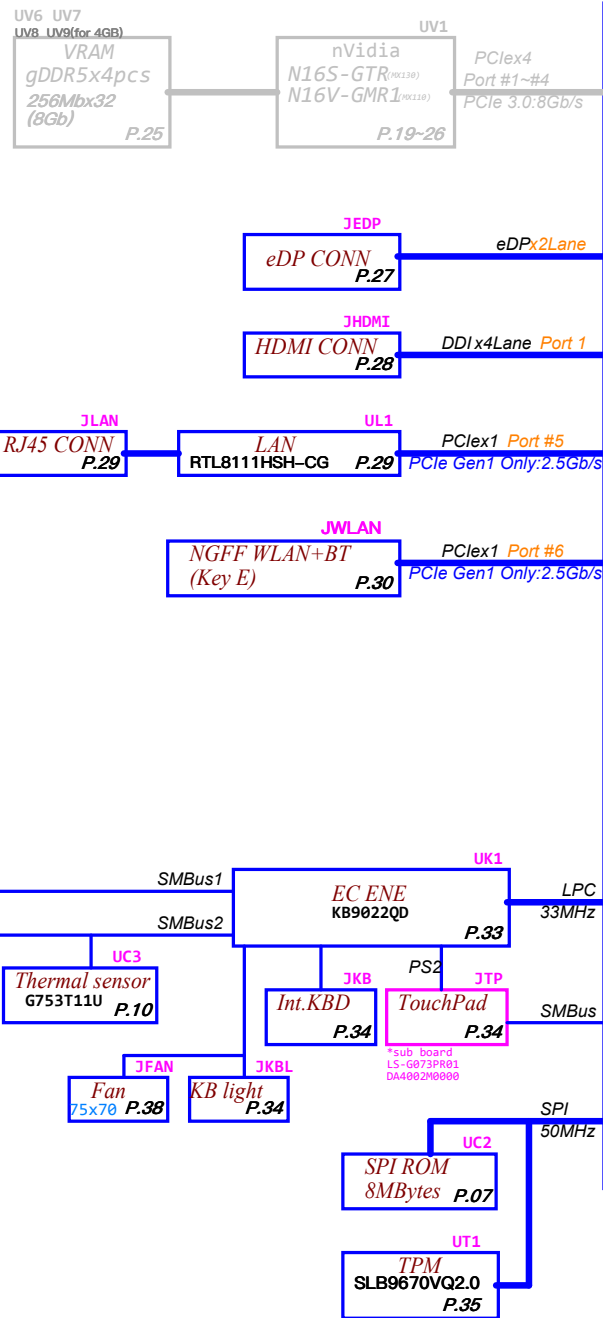
UMA

(Modified&Ref from: 01. "NFLC_KBLR_LAE802PR10_MV_FINAL")

(02. "Canadiens_LA-F035P-R10_KBL-UR_2017-06-23_CPU")

(02. "CNL-U ORB_DDX02_LA-F152PR01_0822B")

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				Rev	v0.3



Kaby Lake-RU42

1356P BGA

UC1

ChA:JIDIMM1(REV)
ChB:JIDIMM2(STD)

DDR4-SO-DIMM X 2
P.17~18

Dual Channel Interleaved
DDR4 2133MHz 1.2V

SATA 3.0 Port 0 JHDD
P.30

2.5" SATA HDD
(sub board)
*sub board
LS-G072P
DA4002LZ000

SATA 3.0 Port 1 JODD
SATA ODD P.30

M.2 SATA SSD
(sub board)
*sub board
LS-G074P
DA6001WR005

PCIe 3.0: 8Gb/s PCIe x2 JSSD
Port #11~#12 M.2 SSD(Key M)
P.19

eMMC
(sub board)
*sub board
LS-G075P
DA6001WS005

SATA 3.0 Port 2

USB3.0
5Gb/s

USB2.0 Port 1 JUSB1
480Mb/s USB3.0 port P.30

Port 2 JUSB2
USB3.0 port P.31

Port 3 JI0
USB2.0 Port P.31

Port 4 JI1
Card Reader P.29

*sub board
LS-G071PR01
DA6001W3000

Port 5 JEDP
Camera P.27

Port 6 JWLAN
Bluetooth P.30

Port 7 JEDP
Touch Screen P.27

HDA 24MHz UA1
HDA Audio codec P.32

JSPK
Internal SPK P.32

JHP
Combo Jack P.32

MB Board Information:
01.DA6001W3000, PCB 29L LS-G071P REV0 I0B(4350M832L01)
02.DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(4350M932L01)
03.DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(4350MA32L01)
04.DA6001W0000, PCB 29M LA-G074P REV0 MB 3(KBLU_2G)
05.DA8001E1000, PCB 29L LA-G078P REV0 MB 3(KBLR_4G)
06.DA6001W1000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
07.DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
08.DA6001Y0000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

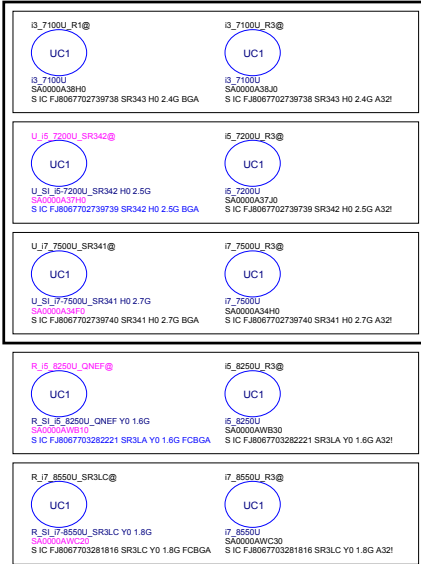
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02.DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(4350M932L01)
03.DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(4350MA32L01)
04.DA6001W0000, PCB 29M LA-G074P REV0 MB 3(KBLU_2G)
05.DA8001E1000, PCB 29L LA-G078P REV0 MB 3(KBLR_4G)
06.DA6001W1000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
07.DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
08.DA6001Y0000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)		Address (8bit)	
			Write	Read	Write	Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1	
		DIMM2	0x52	0xA4	0xA5	
		Touch PAD	0x2C	0x58	0x59	



EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

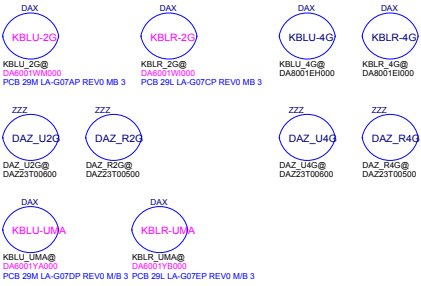
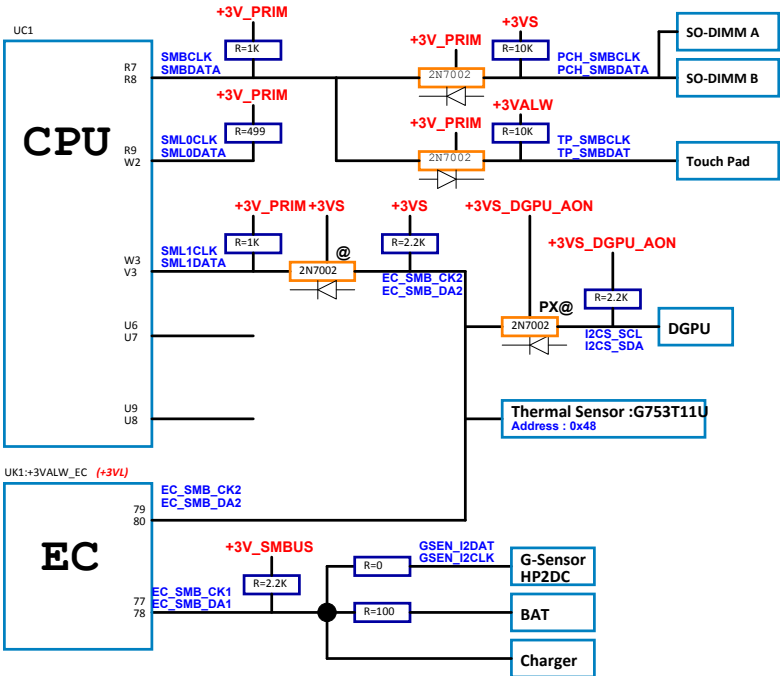
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR 1/IR 2 Camera
6	IR 2 Camera
7	Card Reader
8	X
9	X
10	X

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION	CLK
1			1	USB3.0 Type-C	X
2			2	USB3.0 Type-C	X
3			3	USB2.0/USB3.0	X
4			4	USB2.0/USB3.0	X
5	1		5	GPU(DIS only)	CLK0
6	2		6	GPU(DIS only)	
7	3			GPU(DIS only)	
8	4			GPU(DIS only)	
9	5			LAN	CLK1
10	6			WLAN	CLK2
11	7	0		HDD	X
12	8	1a		ODD	CLK3
13	9			X	X
14	10			X	X
15	11	1b*		NVMe x2	CLK4
16	12	2		SATA SSD	X

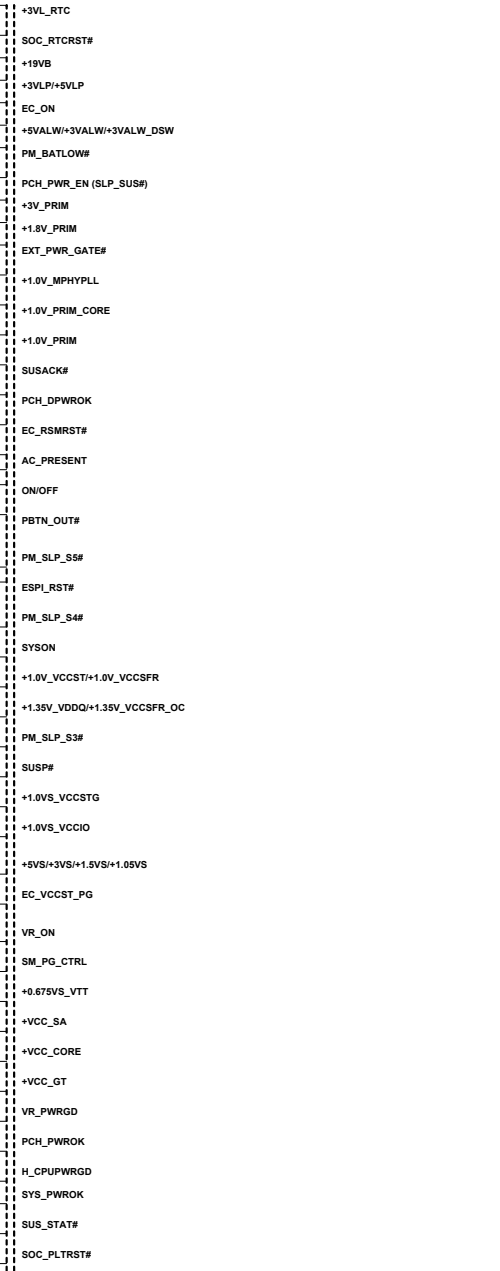
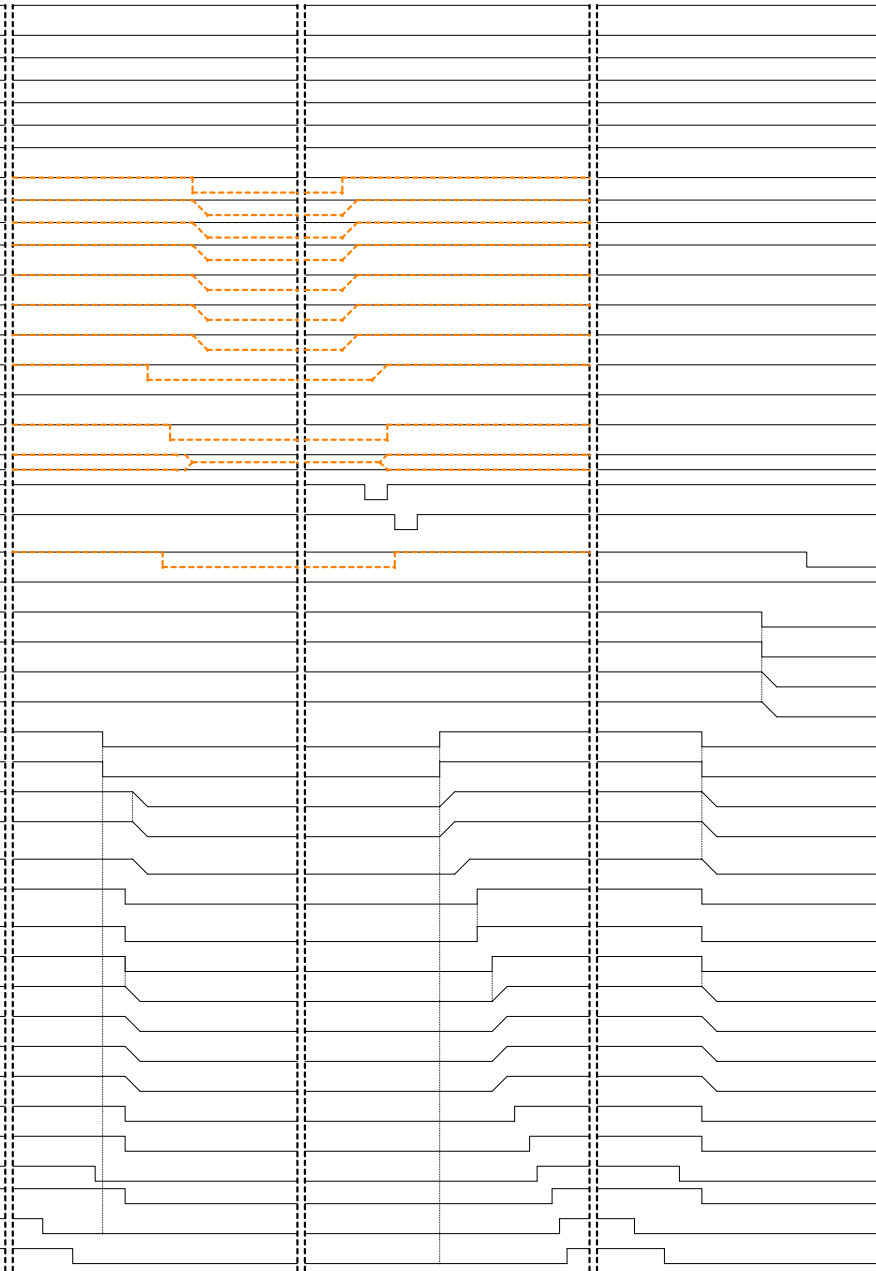
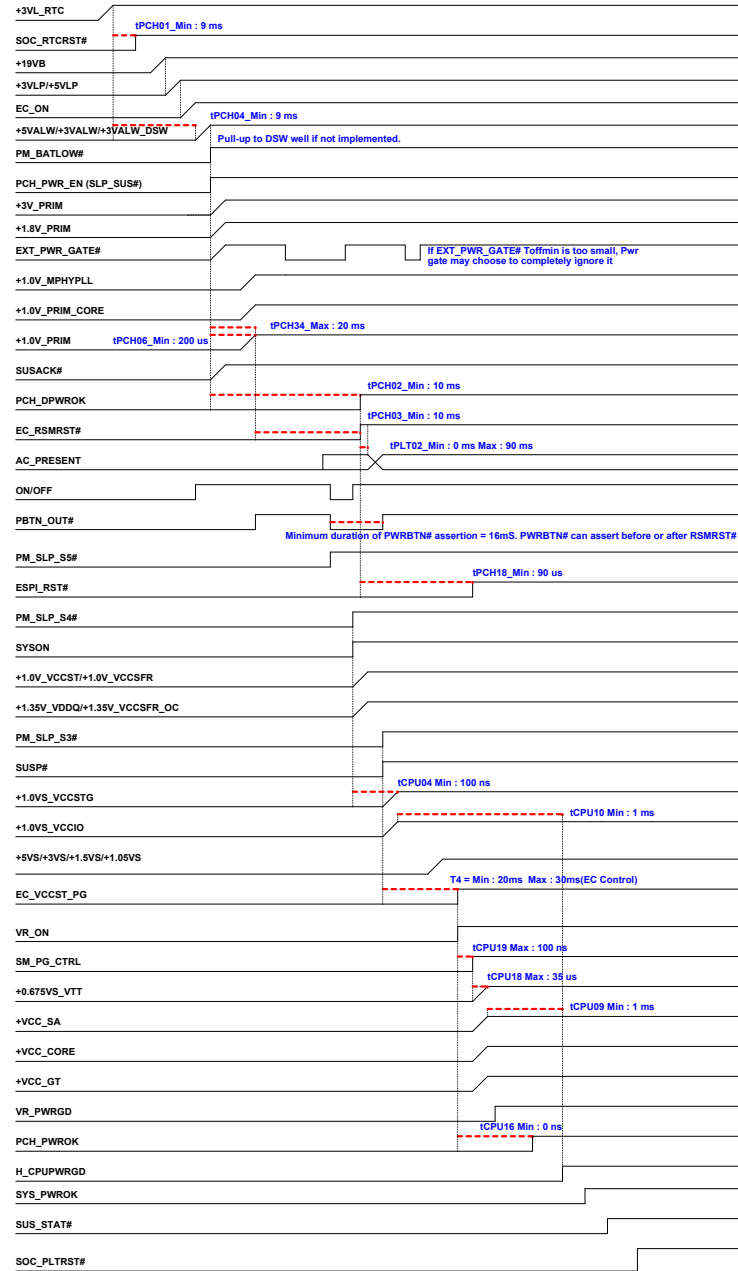


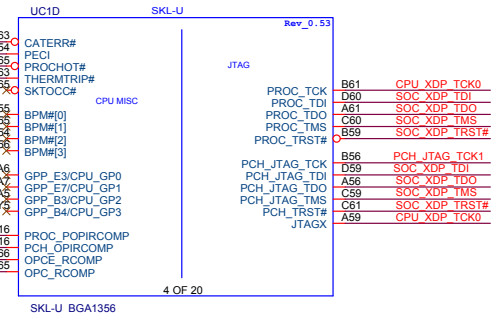
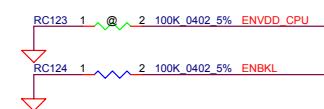
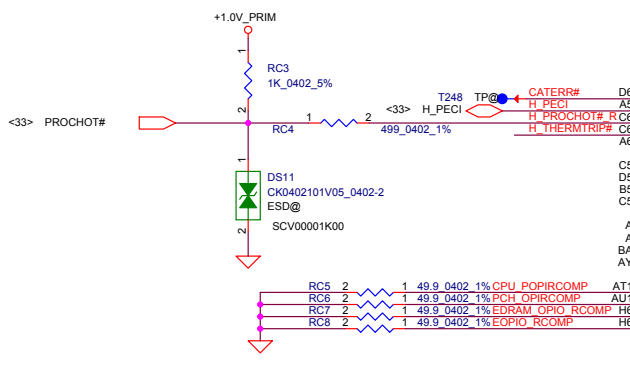
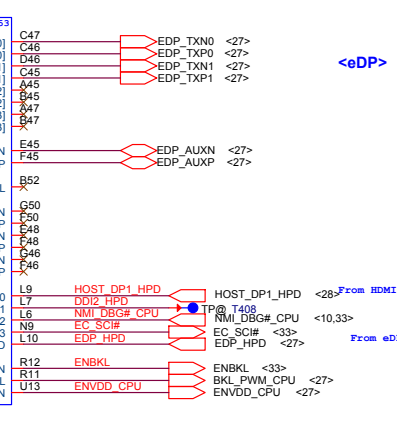
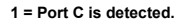
G3->S0

S0->S3/DS3

S0/DS3->S0

S0->S5



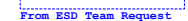


Timing diagram for XDP signals. The diagram shows two signal groups connected to a +1.0V_PRIM supply. The first group includes RC11 (SOC_XDP_TMS), RC13 (SOC_XDP_TDI), RC15 (SOC_XDP_TDO), and RC364 (CPU_XDP_TCK0), all with a period of 1 51 0402 5%. The second group includes RC14 (XDP_PREQ#), RC31 (XDP_ITP_PMODE), RC365 (SOC_XDP_TRST#), RC35 (CPU_XDP_TCK0), RC37 (PCH_JTAG_TCK1), and RC366 (CFG3). RC14 and RC31 have a period of 1 51 0402 5%, while RC365, RC35, and RC37 have a period of 1 51 0402 1%. RC366 has a period of 2 0 0402 5%. The signals are connected to a +1.0V_PRIM supply and a ground symbol. The diagram also shows the SD000008H80 and SD000008H80 memory locations.

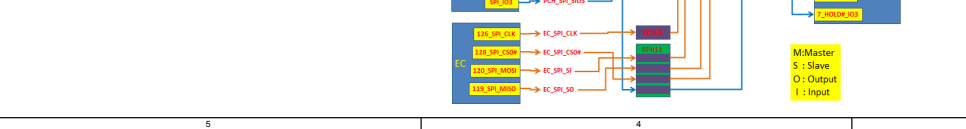
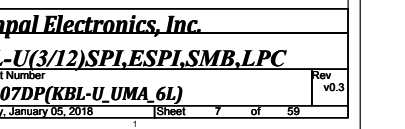
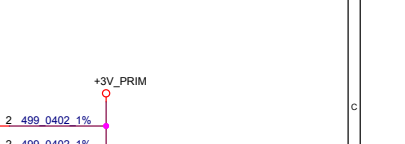
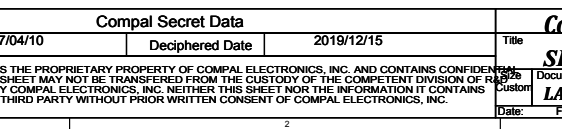
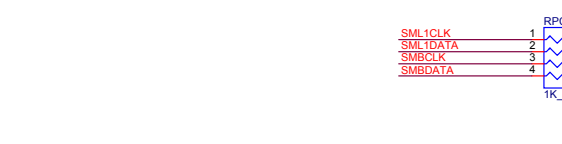
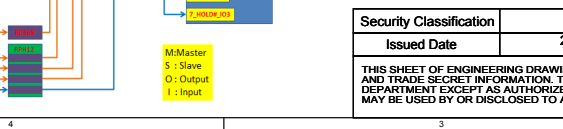
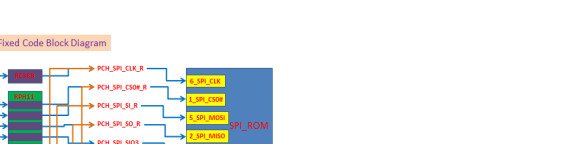
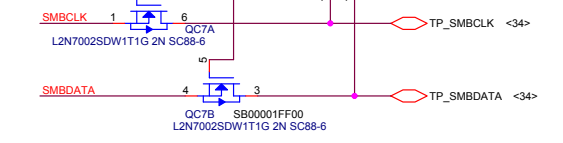
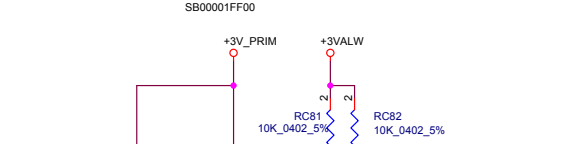
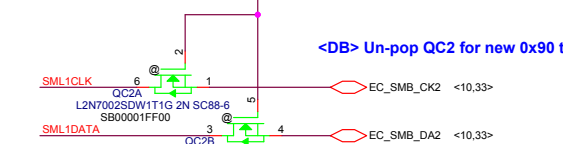
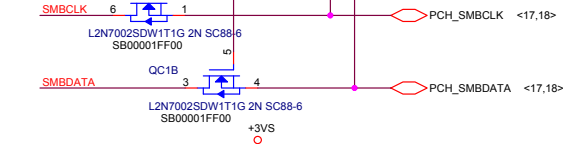
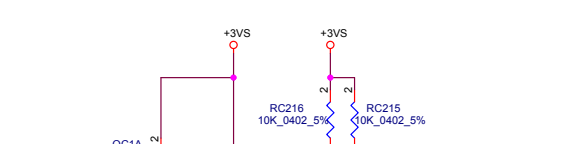
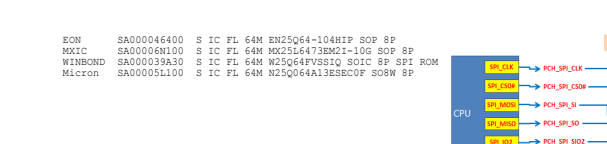
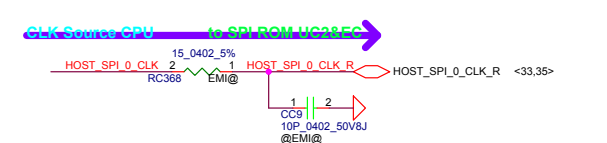
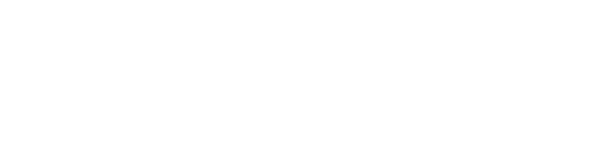
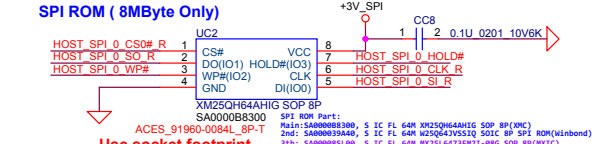
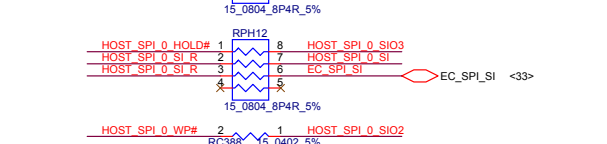
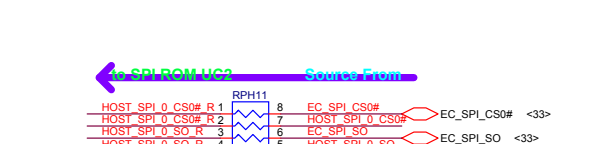
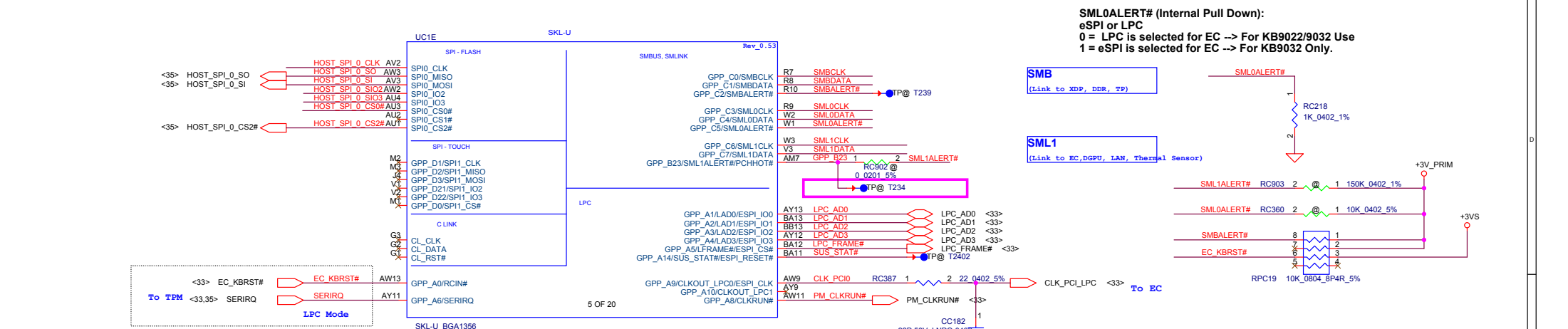
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Interleaved Memory

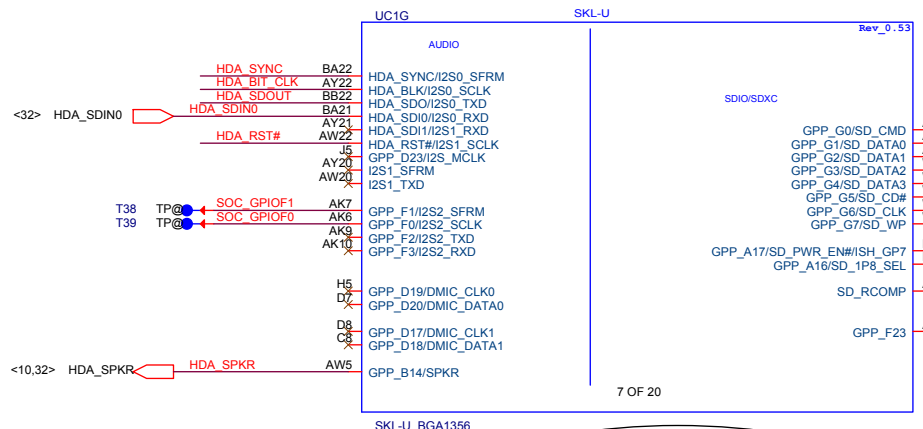
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ (Memory down); FET+R (SO-DIMM)



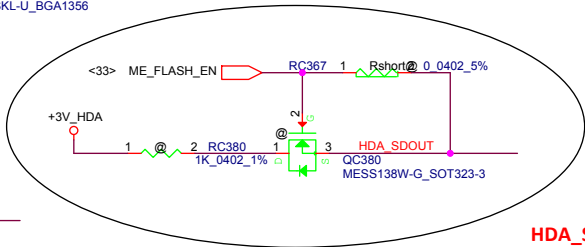
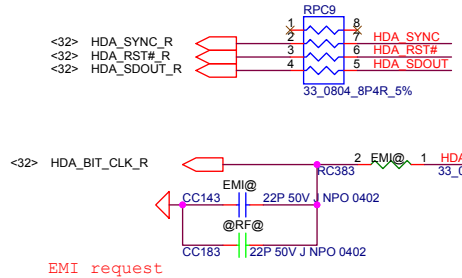
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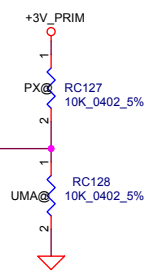
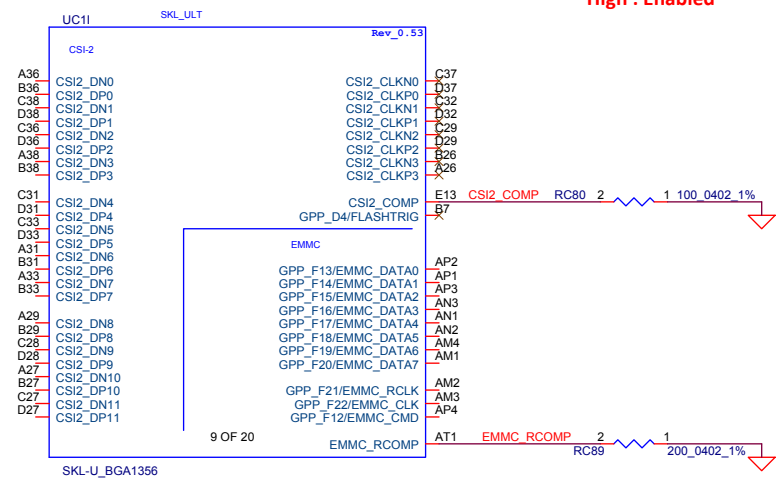
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Issued Date	2017/04/10	Deciphered Date	2019/12/15	SKL-U(3/12)SPI,ESPI,SMB,LPC	
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Date: Friday, January 05, 2018				Sheet 7	of 59



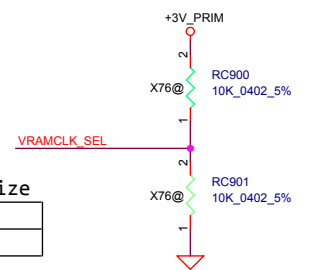
HDA for AUDIO



HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled

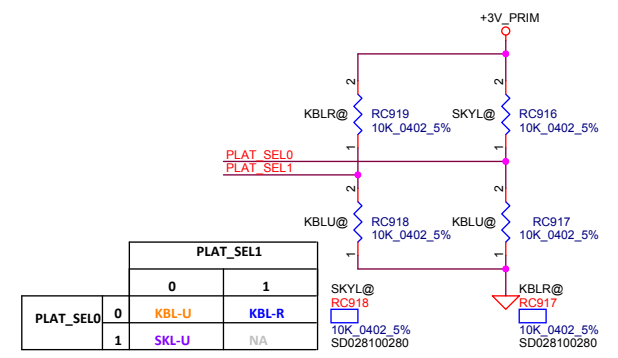


	UMA	DIS
PROJECT_ID	0	1
VRAM Clock	0	1

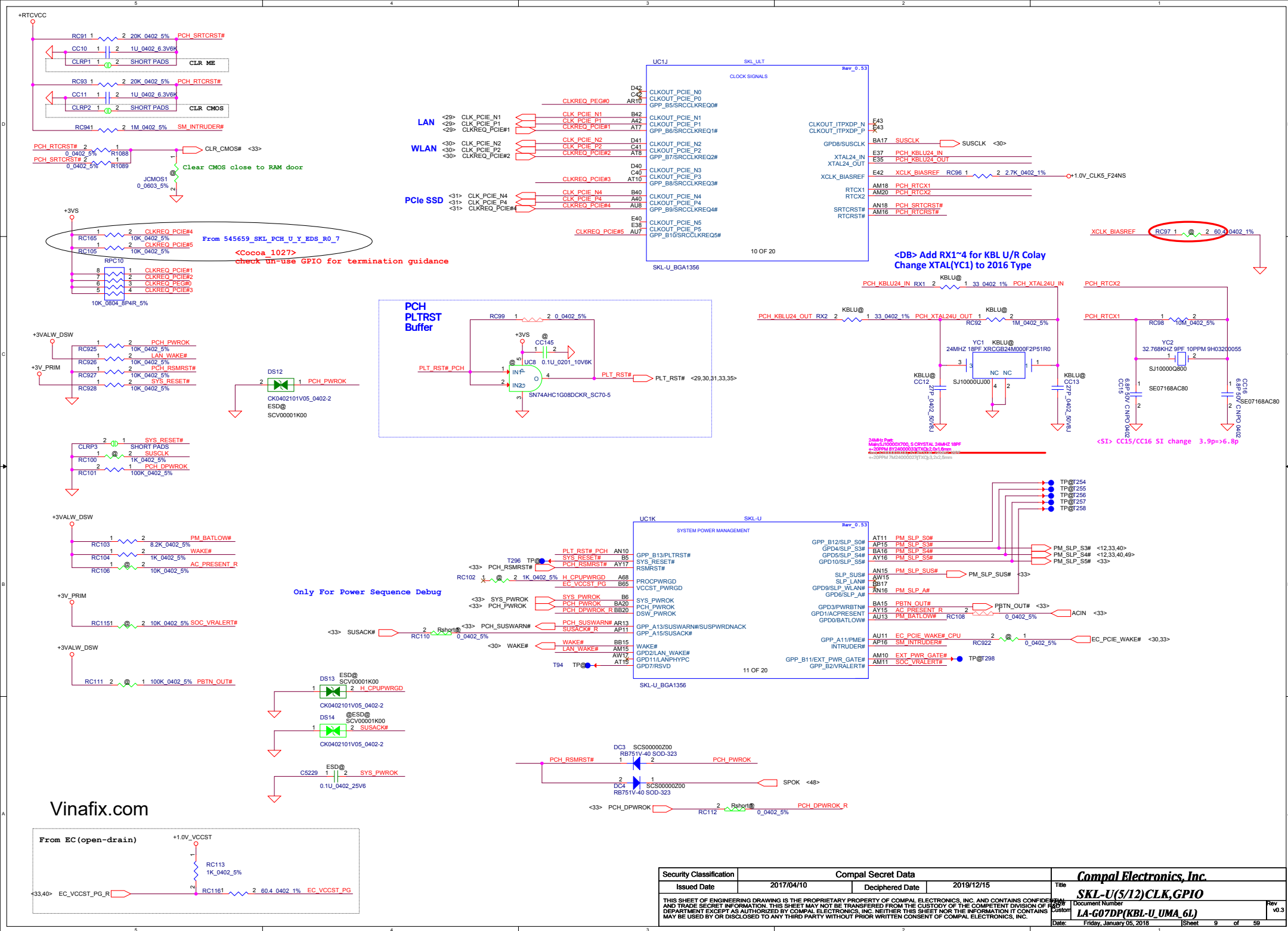


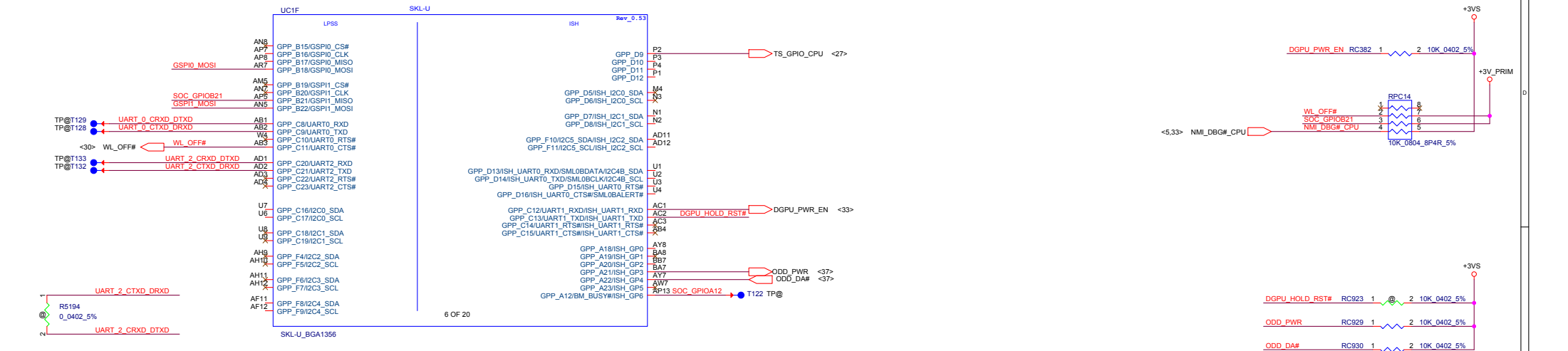
X76 BOM control RAM size

Net Name	4G	2G
VRAMCLK_SEL	1	0

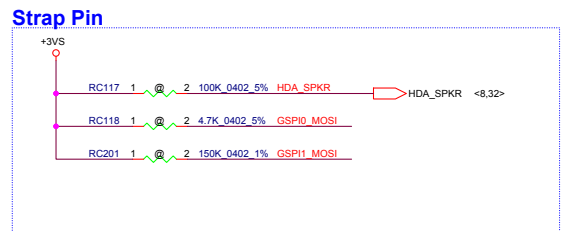


		PLAT_SEL1	
		0	1
PLAT_SEL0	0	KBL-U	KBL-R
	1	SKL-U	NA

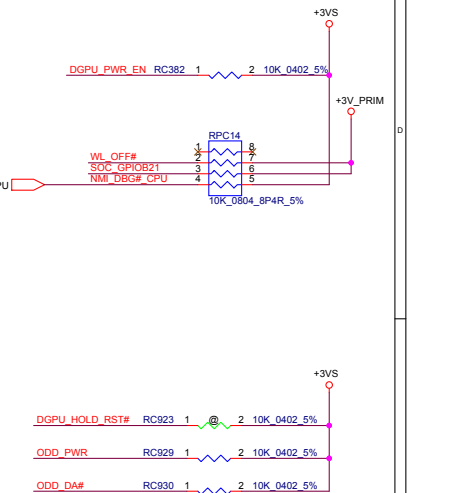
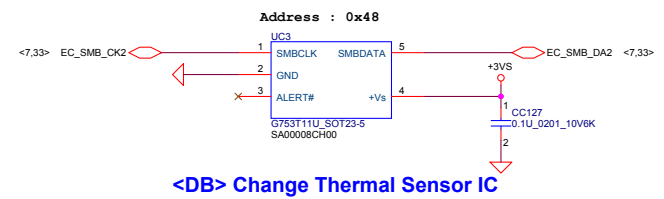




- Functional Strap Definitions**
- SPKR (Internal Pull Down):**
- TOP Swap Override**
- 0 = Disable TOP Swap mode.----> AAX05 Use
- 1 = Enable TOP Swap Mode.
- GSPI0_MOSI (Internal Pull Down):**
- No Reboot**
- 0 = Disable No Reboot mode. --> AAX05 Use
- 1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
- GSPI1_MOSI (Internal Pull Down):**
- Boot BIOS Strap Bit**
- 0 = SPI Mode --> AAX05 Use
- 1 = LPC Mode



CPU THERMAL SENSOR



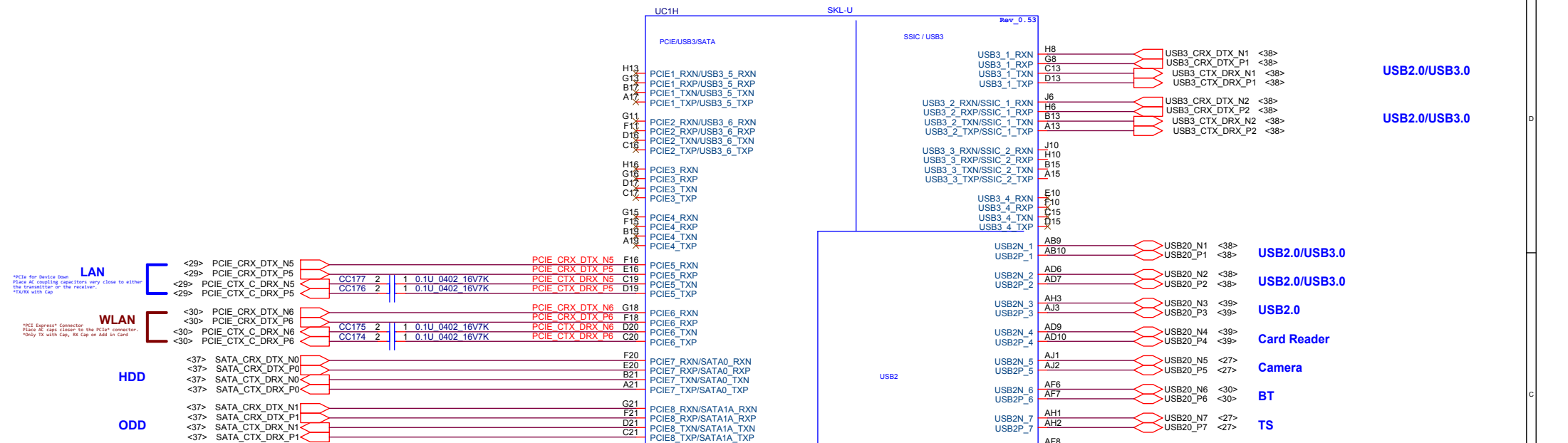
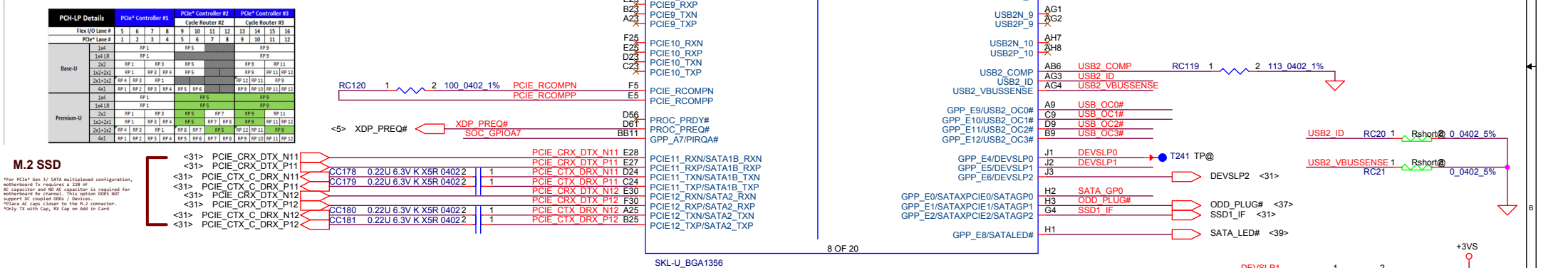
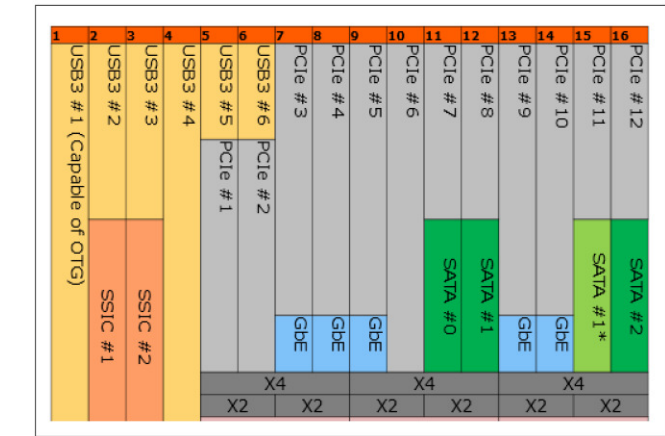


Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter



High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

+1.2V_VDDQ

+1.35V_VDDQ_CPU

Security Classification

Compal Secret Data			
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Title

SKL-U(8/12)Power

Document Number

LA-G07DP(KBL-U_UMA_6L)

Date

Friday, January 05, 2018

Sheet

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Rev

v0.3

[illegible]

+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

+1.2V_VDDQ

+1.35V_VDDQ_CPU

UC1N SKL-U Rev_0_53

SKL-U BGA1356

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RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev1.0

RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53

CC47 Follow 543016_SKL_U_V_PDG_0_9

**+1.35V_VDDQ_CPU : 10UF/6.3V/0603 * 6
1UF/6.3V/0402 * 4**

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								LA-G07DP(KBL-U_UMA_6L)		v0.3	
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+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

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Security Classification: Compal Secret Data
Issued Date: 2017/04/10
Deciphered Date: 2019/12/15
Title: SKL-U(8/12)Power
Document Number: LA-G07DP(KBL-U_UMA_6L)
Date: Friday, January 05, 2018
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+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

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+1.0V_PRIM TO +1.0V_VCCSTU

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

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+1.0V_VCCSTU

+1.2V_VDDQ

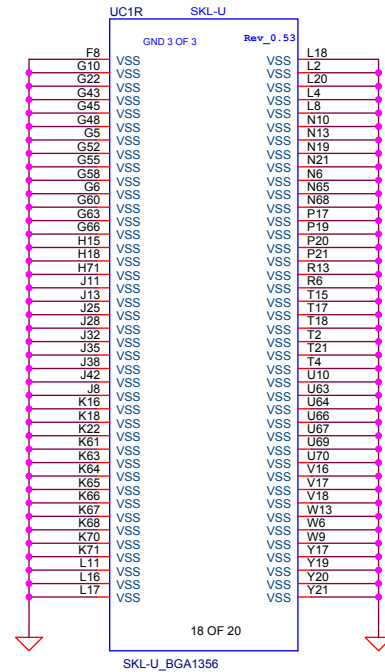
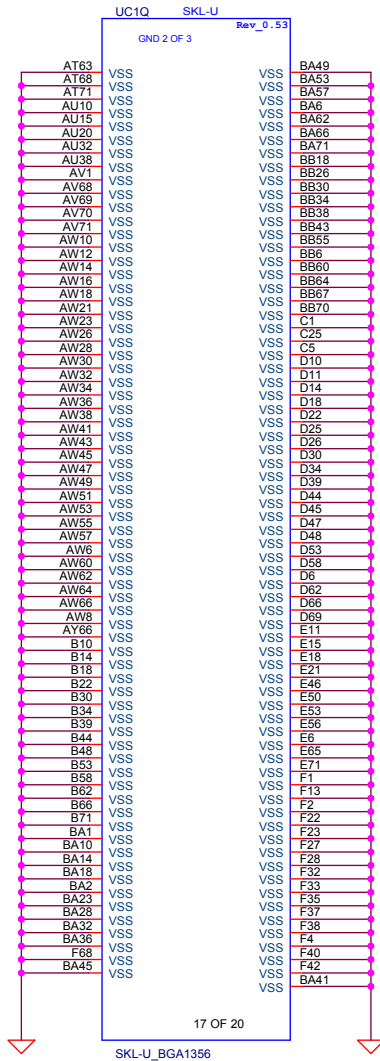
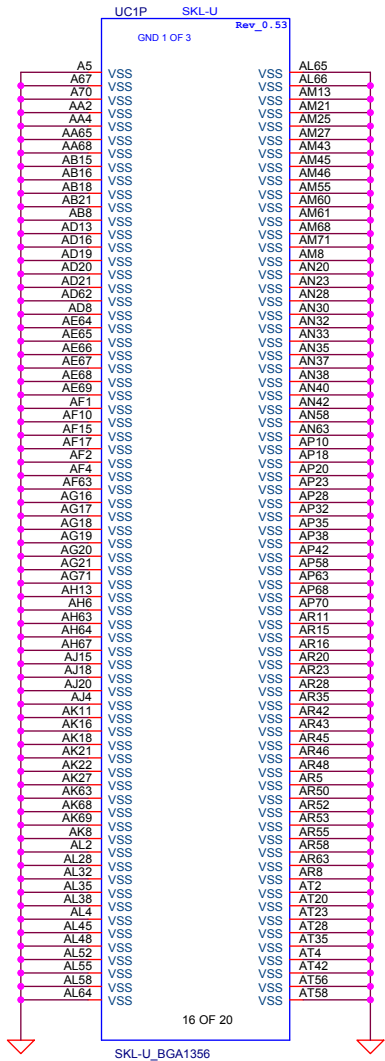
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Date:								Friday, January 05, 2018		Sheet 12 of 59	



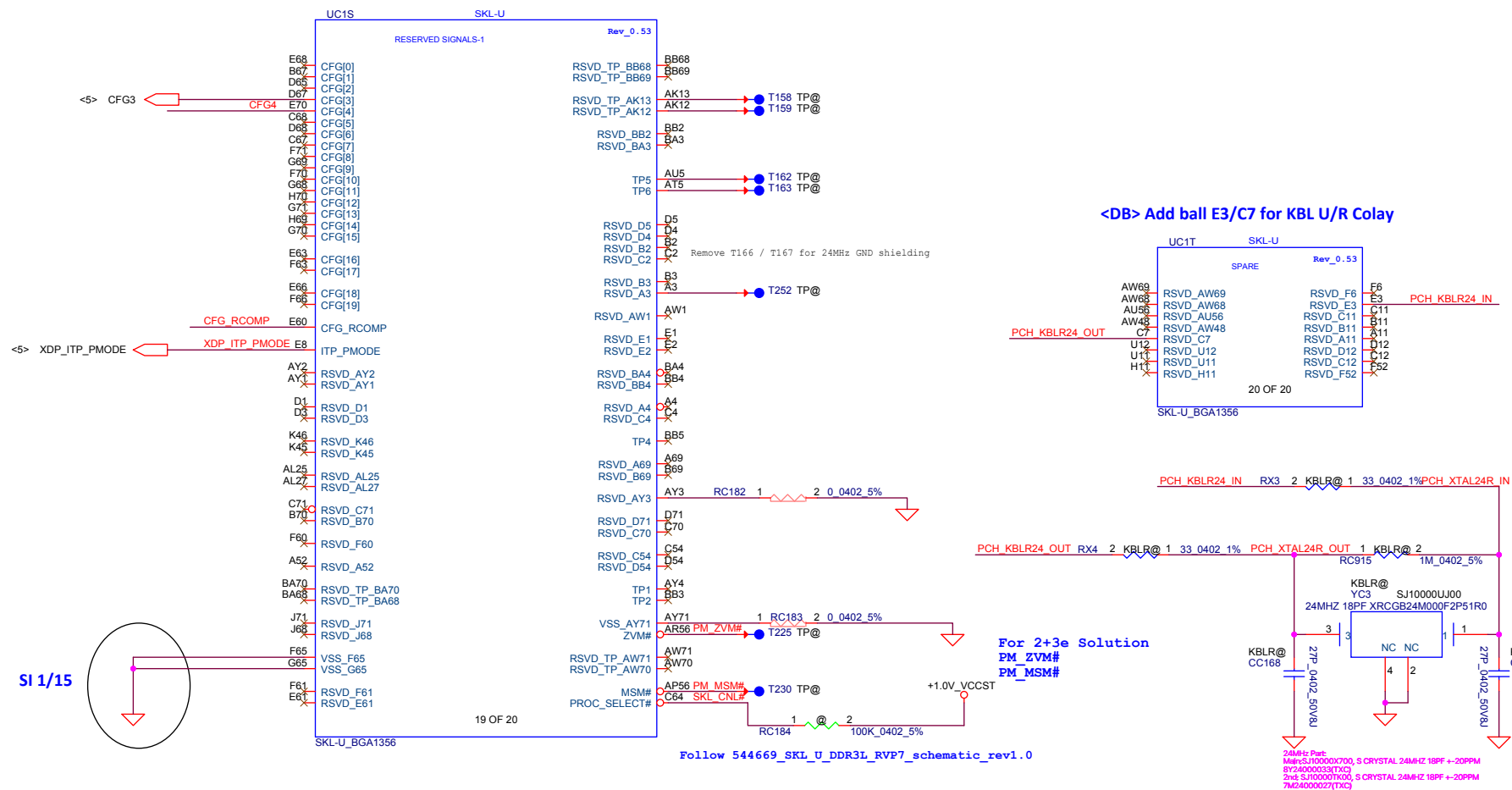
Must Not Be Connected. RVP use this signal for debug and testing purpose only.

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SKL-U(10/12)Power,SVID	
Document Number	Rev
LA-G07DP(KBL-U_UMA_6L)	v0.3



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Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

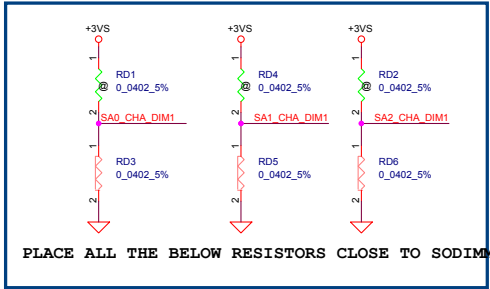
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						Document Number				
						LA-G07DP(KBL-U UMA 6L)				
						Rev v0.3				
Date:		Friday, January 05, 2018		Sheet 16 of 59						

CHANNEL-A

REVERSE TYPE

Interleaved Memory

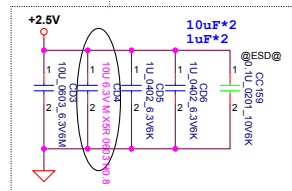
TOP: JDIMM1 CONN Non-ECC DIMM



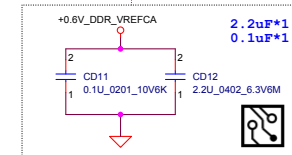
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

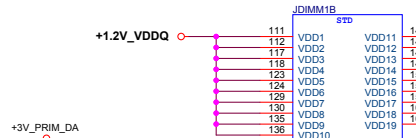
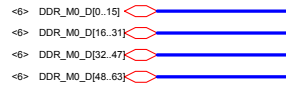
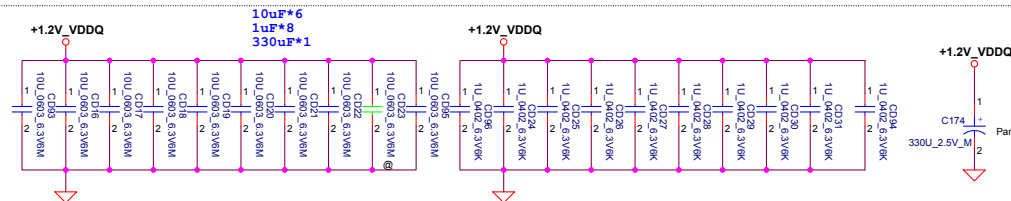
Layout Note:
Place near JDIMM1.258



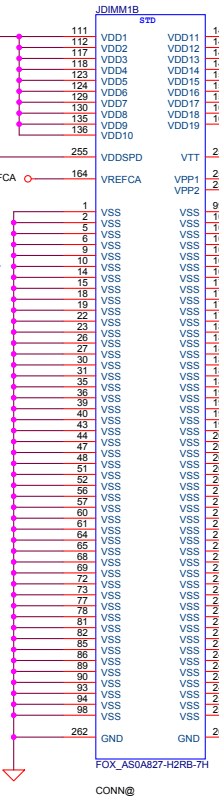
Layout Note:
PLACE THE CAP near JDIMM1.164



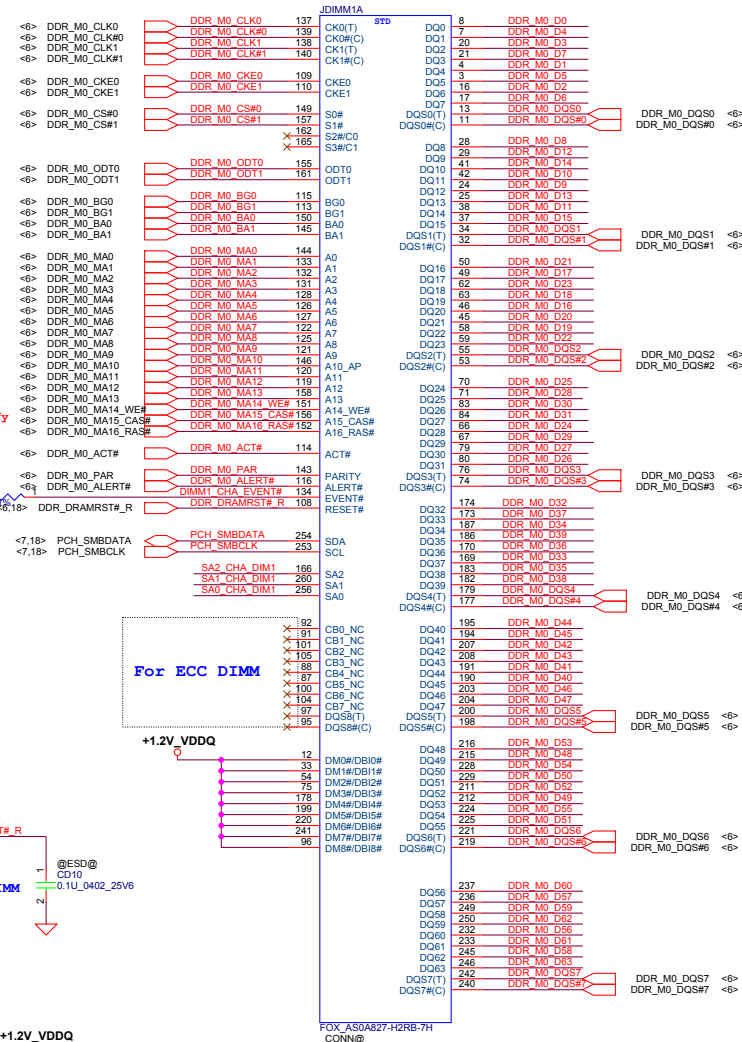
Layout Note:
Place near JDIMM1



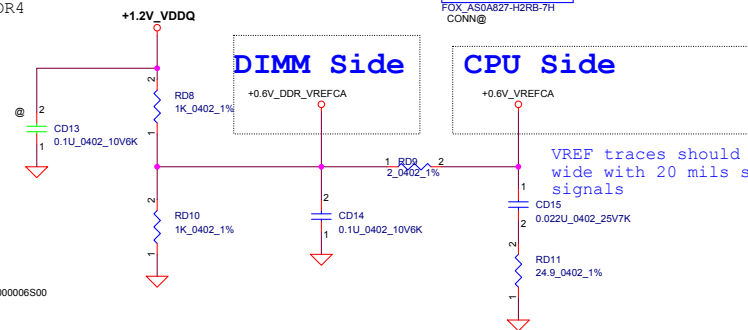
PLACE NEAR TO PIN



Part Number: LTCX0069GA0
Part Value: S SOCKET FOX AS0A827-H2RB-7H 260P DDR4



PLACE NEAR TO SODIMM

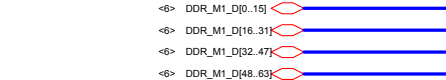


VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Interleaved Memory

TOP: JDIMM2 CONN Non-ECC DIMM



Pinout diagram for the J101 connector:

Pin Number	Signal Name
111	+1.2V_VDDQ
112	VDD0
117	VDD2
118	VDD3
123	VDD4
124	VDD5
129	VDD6
130	VDD7
135	VDD8
136	VDD9
136	+3V3_PRIM_DB

Connector: J101MM2B
Standard: STD

0.1µF CD60

2.2µF CD61

0.6V_VDDRB_VREFCA

255 VDDSPD

164 VREFCA

1 VSS

2 VSS

3 VSS

4 VSS

5 VSS

6 VSS

7 VSS

8 VSS

9 VSS

10 VSS

11 VSS

12 VSS

13 VSS

14 VSS

15 VSS

16 VSS

17 VSS

18 VSS

19 VSS

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153 VSS

154 VSS

155 VSS

156 VSS

157 VSS

158 VSS

159 VSS

160 VSS

161 VSS

162 VSS

163 VSS

164 VREFCA

165 VREFCA

166 VREFCA

167 VREFCA

168 VREFCA

169 VREFCA

170 VREFCA

171 VREFCA

172 VREFCA

173 VREFCA

174 VREFCA

175 VREFCA

176 VREFCA

177 VREFCA

178 VREFCA

179 VREFCA

180 VREFCA

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254 VREFCA

255 VDDSPD

256 VDDSPD

257 VDDSPD

258 VDDSPD

259 VDDSPD

260 VDDSPD

261 VDDSPD

262 VDDSPD

263 VDDSPD

264 VDDSPD

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266 VDDSPD

267 VDDSPD

268 VDDSPD

269 VDDSPD

270 VDDSPD

271 VDDSPD

272 VDDSPD

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305 VDDSPD

306 VDDSPD

307 VDDSPD

308 VDDSPD

309 VDDSPD

310 VDDSPD

311 VDDSPD

312 VDDSPD

313 VDDSPD

314 VDDSPD

315 VDDSPD

316 VDDSPD

317 VDDSPD

318 VDDSPD

319 VDDSPD

320 VDDSPD

321 VDDSPD

322 VDDSPD

323 VDDSPD

324 VDDSPD

325 VDDSPD

326 VDDSPD

327 VDDSPD

328 VDDSPD

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333 VDDSPD

334 VDDSPD

335 VDDSPD

336 VDDSPD

337 VDDSPD

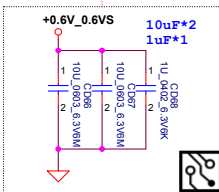
338 VDDSPD

339 VDDSPD

340 VDDSPD

341 VDDSPD</

Layout Note:
Place near JDIMM2.258



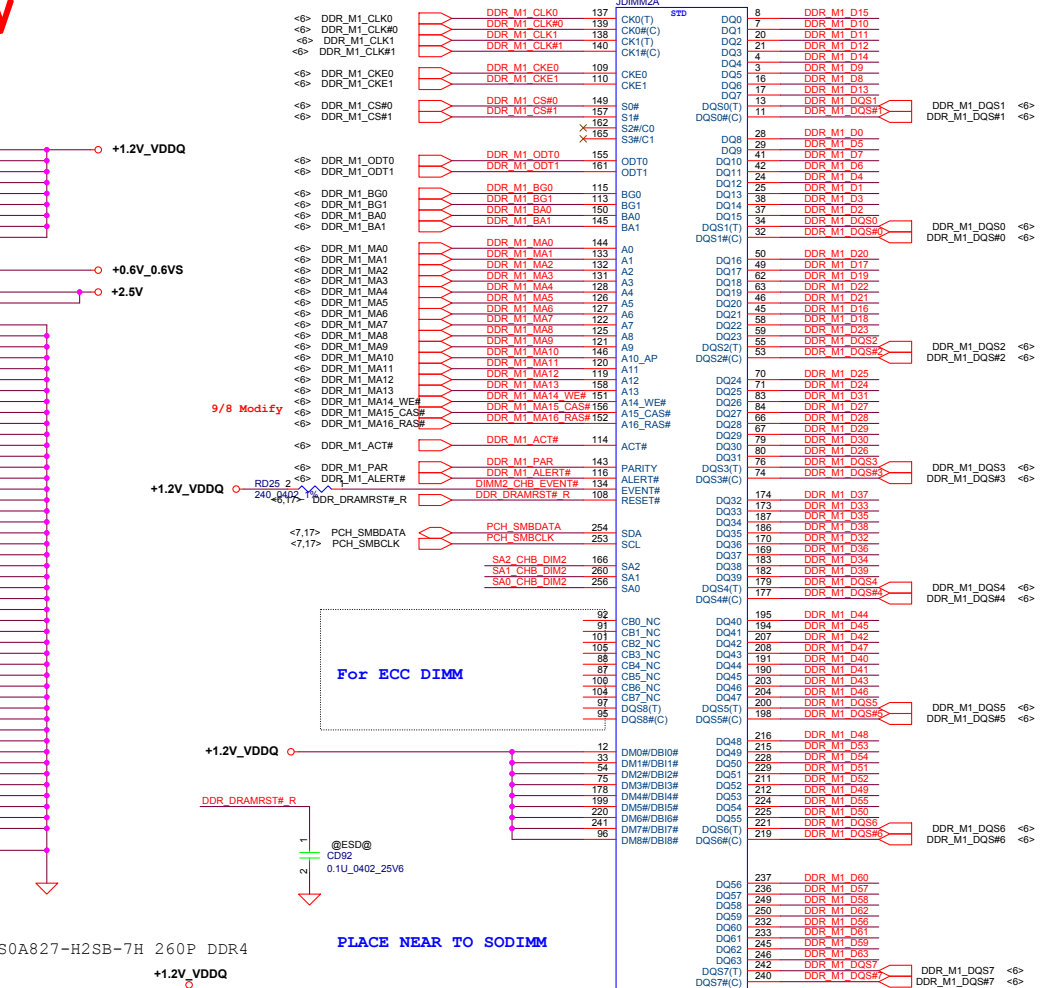
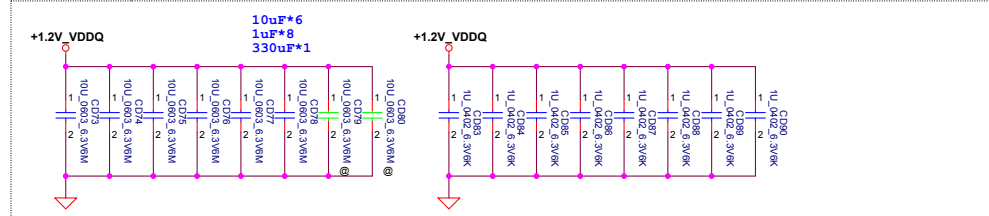
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0.1uF*1

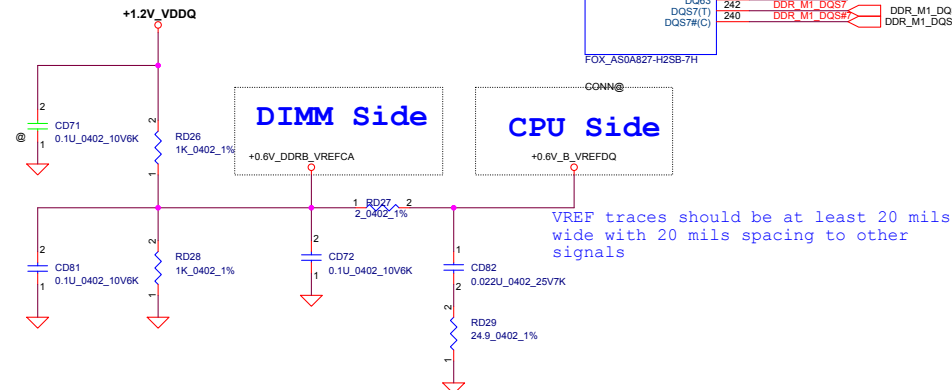
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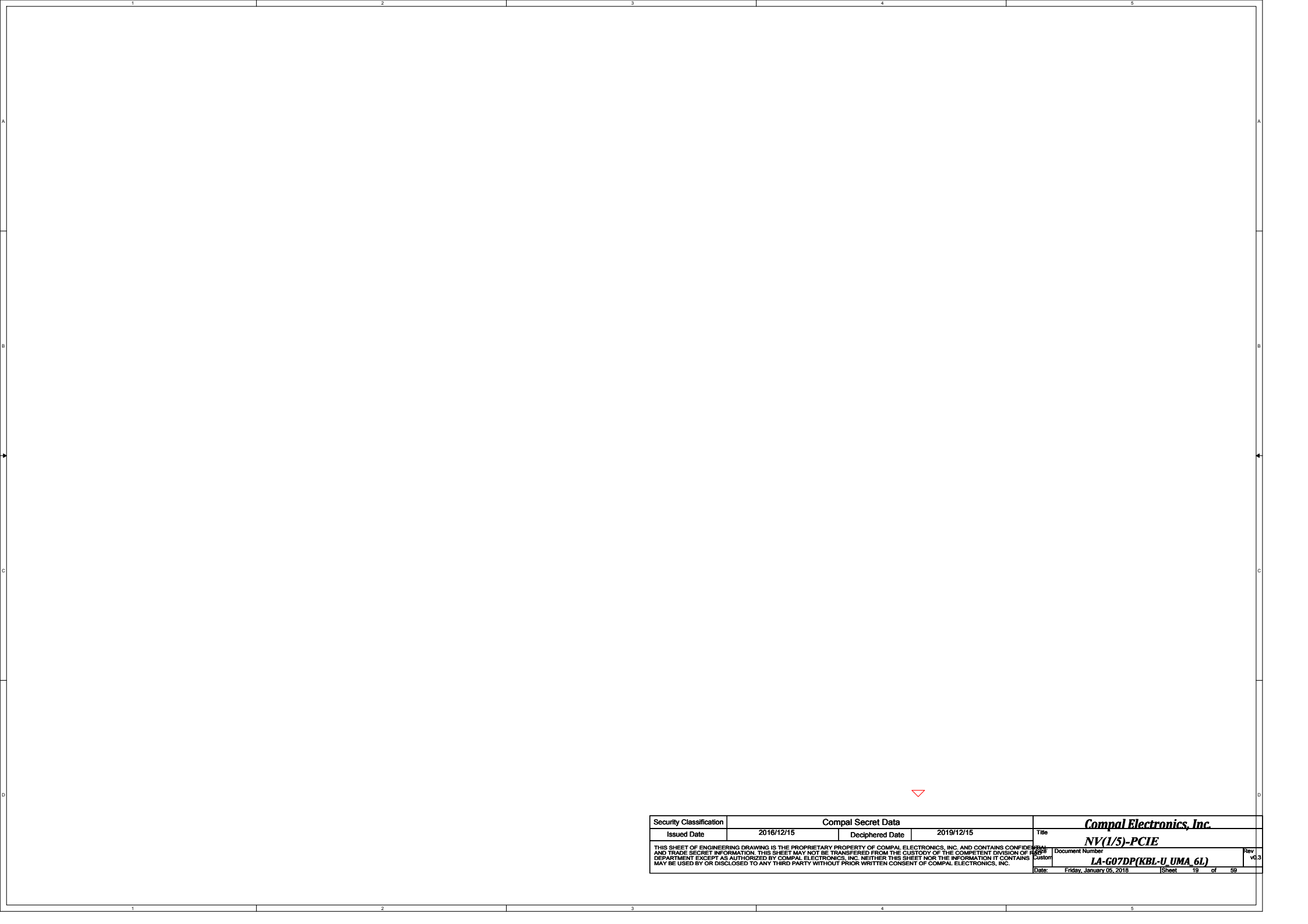
Vinafix.com



PLACE NEAR TO SODIMM



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				LA-G07DP(KBL-U UMA 6L)		v0.3
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				Date: Friday, January 05, 2018	Sheet 19 of 59

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				LA-G07DP(KBL-U_UMA_6L)	V0.3
				Date	Friday, January 05, 2019
				Sheet	20 of 69

1	2	3	4	5
A				A
B				B
C				C
D				D

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				Rev	v0.3
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				Sheet	21 of 59

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Date: Friday, January 05, 2018			Sheet 22 of 59	

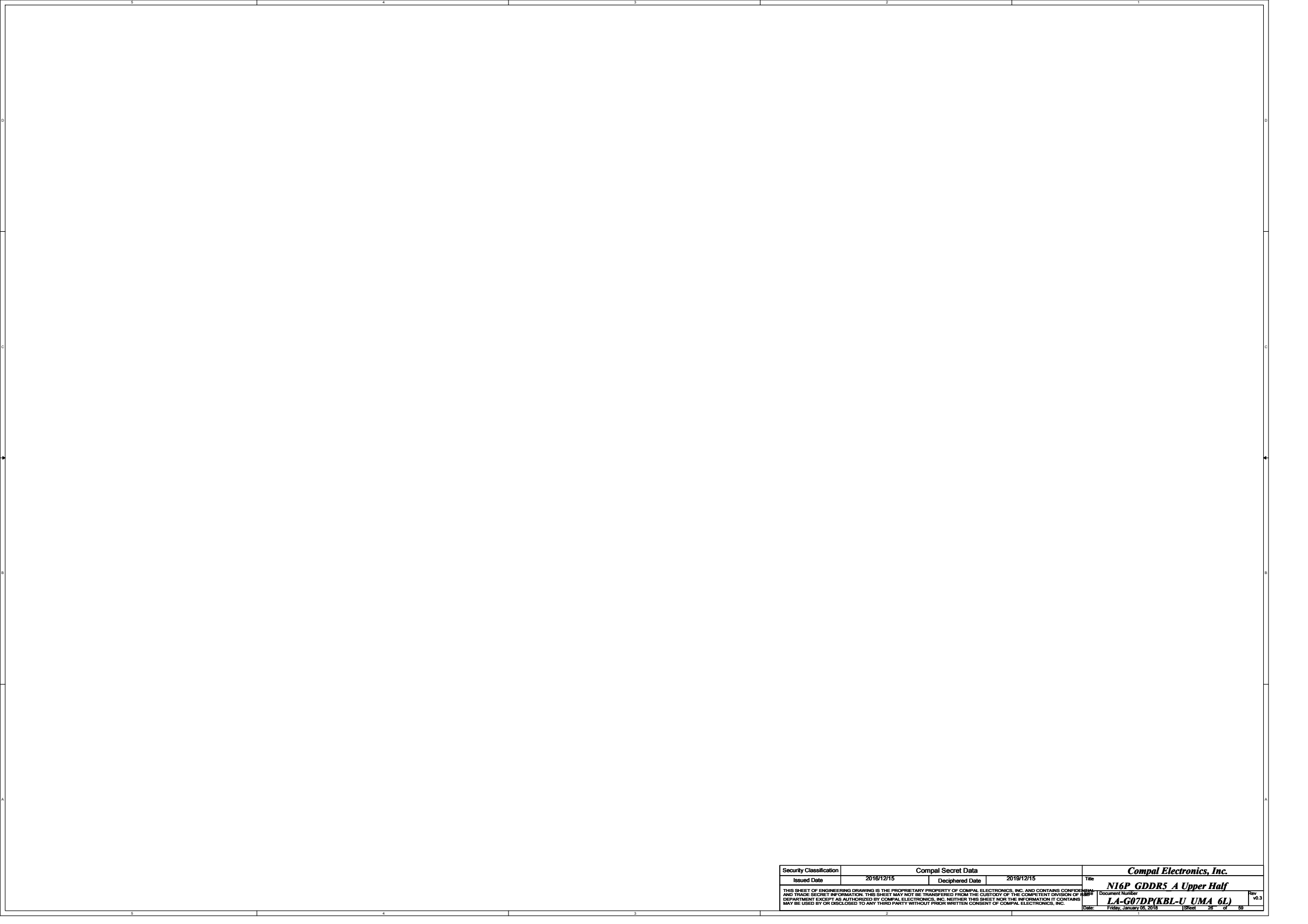
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Issued Date	2016/12/15	Deciphered Date	2019/12/15	NY(5/S)-MEMORY FBA	
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B				B
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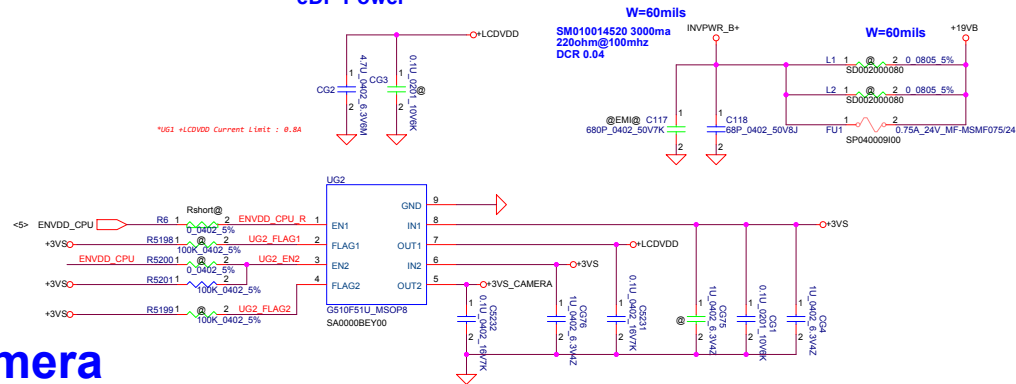
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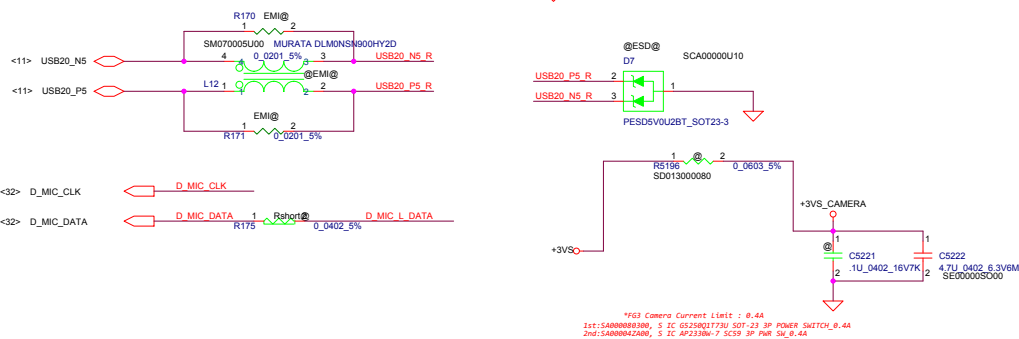


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				Rev
				v0.3
				Date
				Friday, January 05, 2018
				Sheet
				25
				of
				59

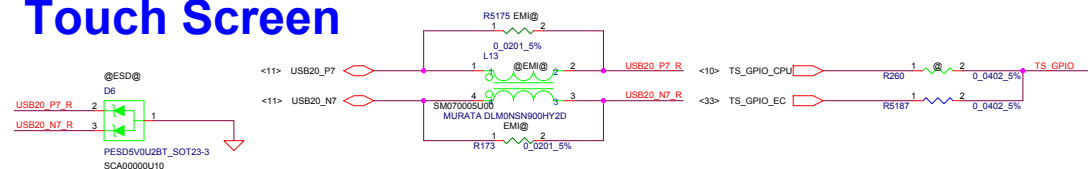
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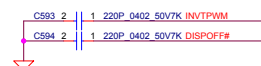
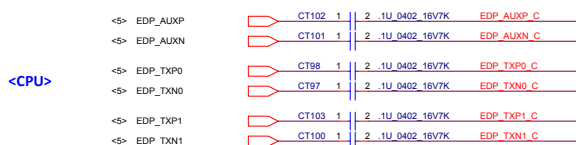
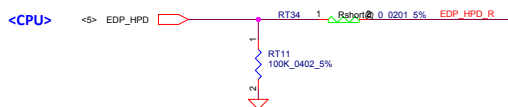
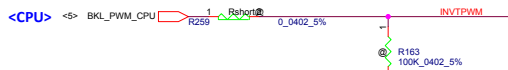
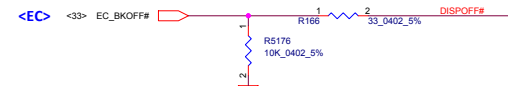
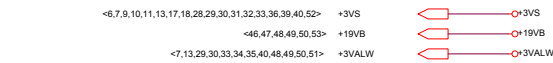
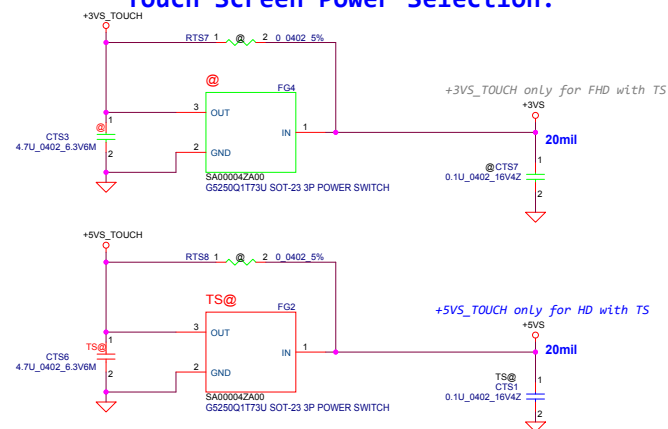
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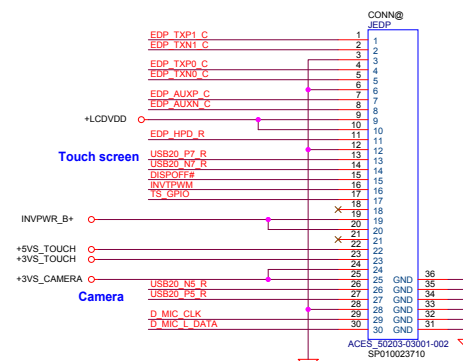
Touch Screen



Touch Screen Power Selection:



eDP



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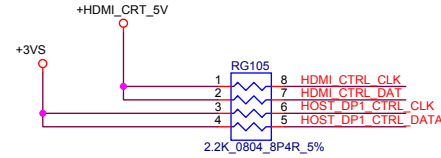
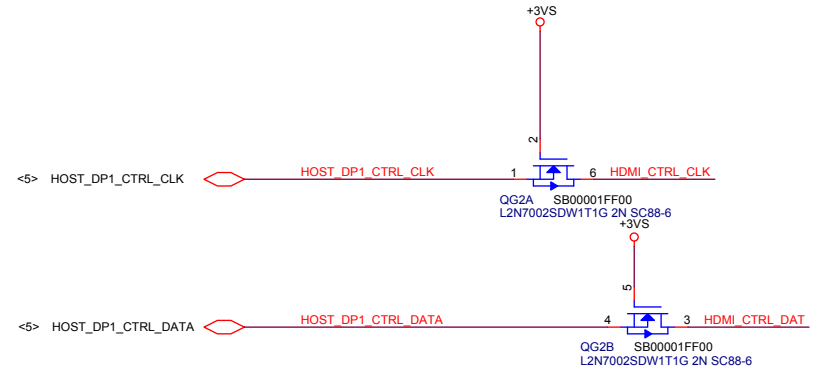
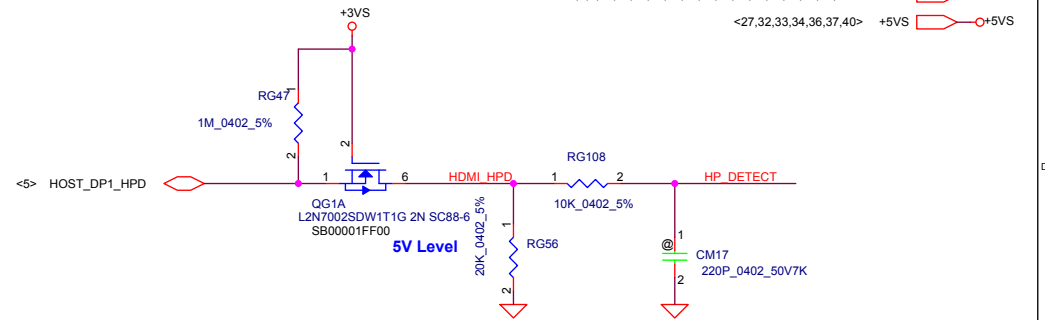
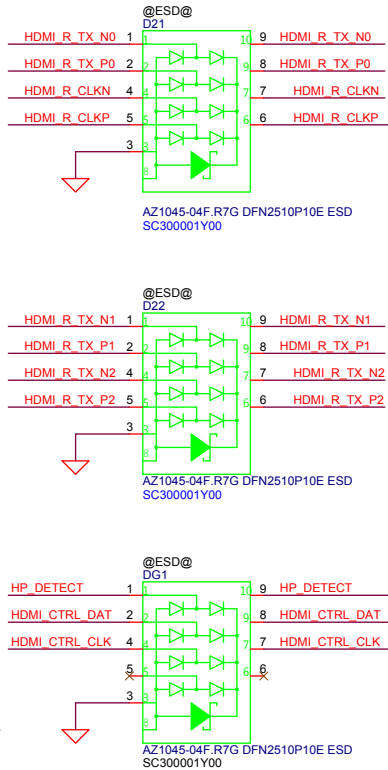
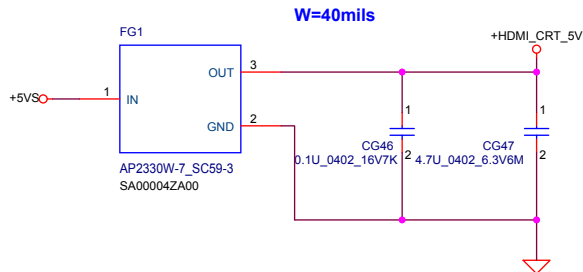
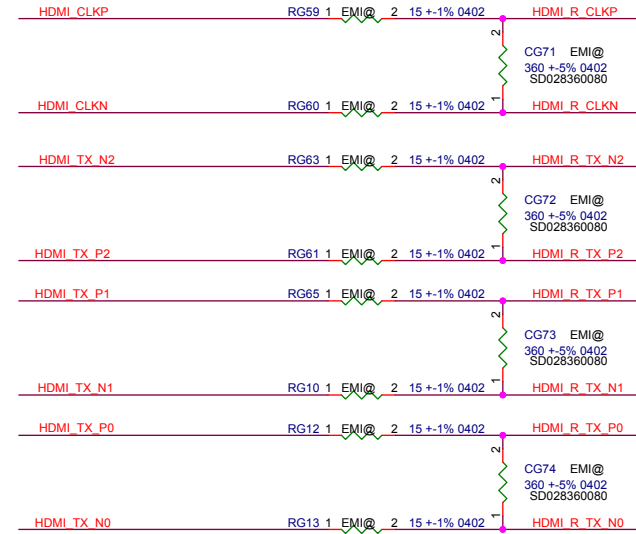
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1.3.2 Digital Display Interface Signal Mapping

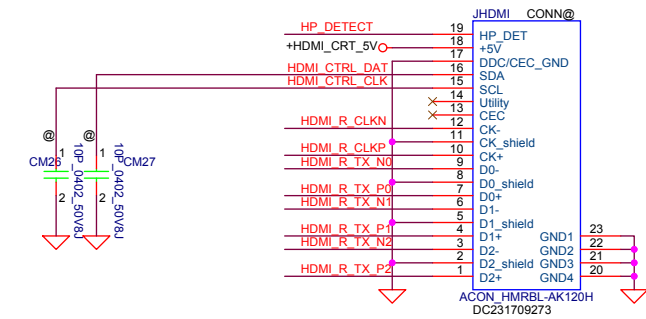
Table 1-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMI_KC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMI_KC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMI_KC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMI_KC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMI_KC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMI_KC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMI_KC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMI_KC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CLK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

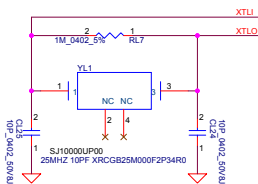
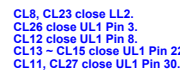
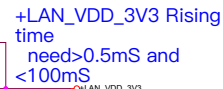
*DDA30_LA-F292PR02: RS_8.2ohm_RP_360ohm



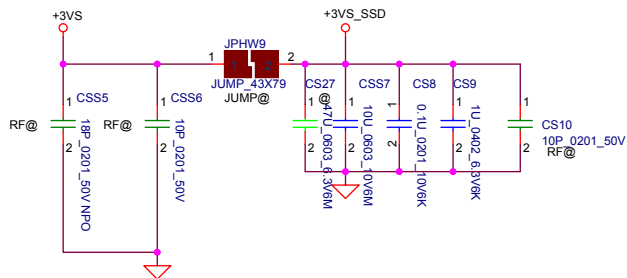
HDMI Conn.



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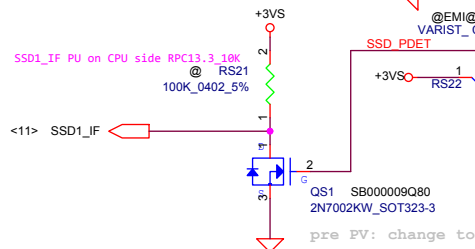
Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details	PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #	5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #	1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1			RP 5				RP 9			
	1x4 LR	RP 1			RP 5				RP 9			
	2x2	RP 1	RP 3	RP 4	RP 5				RP 9	RP 11	RP 12	
	1x2+2x1	RP 1	RP 3	RP 4	RP 5				RP 9	RP 11	RP 12	
	2x1+1x2	RP 4	RP 3	RP 1	RP 5	RP 6			RP 12	RP 11	RP 9	
Premium-U	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11
	1x4	RP 1			RP 5				RP 9			
	1x4 LR	RP 1			RP 5				RP 9			
	2x2	RP 1	RP 3	RP 4	RP 5	RP 7	RP 8		RP 9	RP 11	RP 12	
	1x2+2x1	RP 1	RP 3	RP 4	RP 5	RP 7	RP 8		RP 9	RP 11	RP 12	

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Key TYP. M

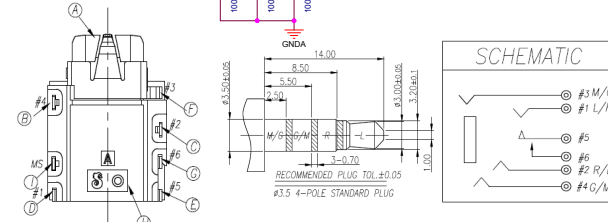
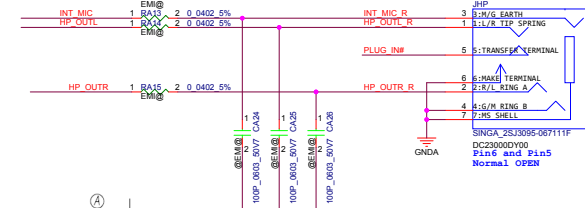
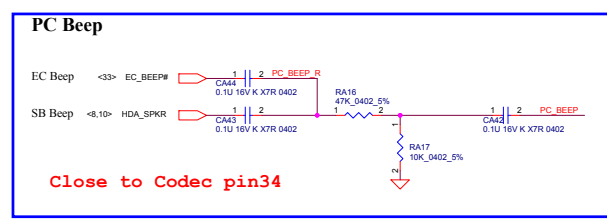
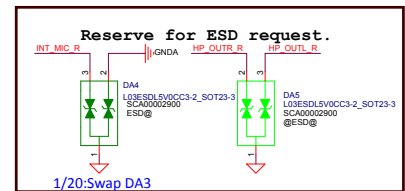
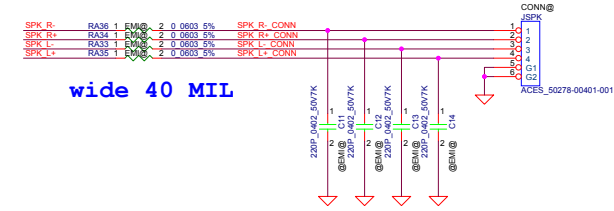
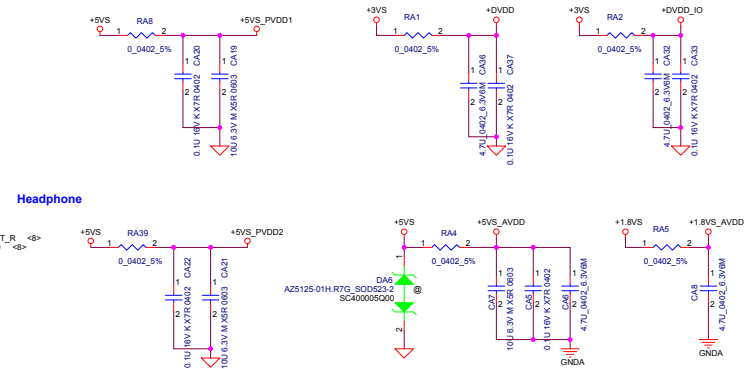
39	GND	PCIeM/Mo_D09000NU90_MZVLW10HMLH-009H1_F73H1Q_0FH	39	GND	Return Current Path	40	GND	Return Current Path
41	PETn0	PCIe TX	42	N/C		41	TXP	Transmitter Differential Signal Pair
43	PETn1	PCIe TX	44	N/C		43	TXN	Transmitter Differential Signal Pair
45	GND	Return current path	46	N/C		45	GND	Return Current Path
47	PERn0	PCIe Rx	48	N/C		47	RXP	Receiver Differential Signal Pair
49	PERn1	PCIe Rx	50	PERST#		49	RXP	Receiver Differential Signal Pair
51	GND	Return current path	52	CLKREQ#		51	GND	Return Current Path

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

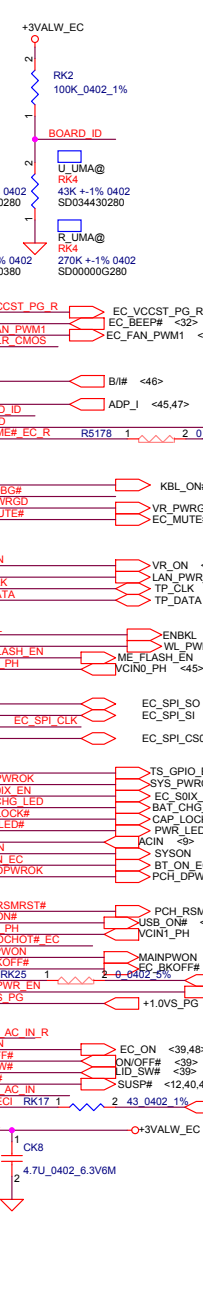
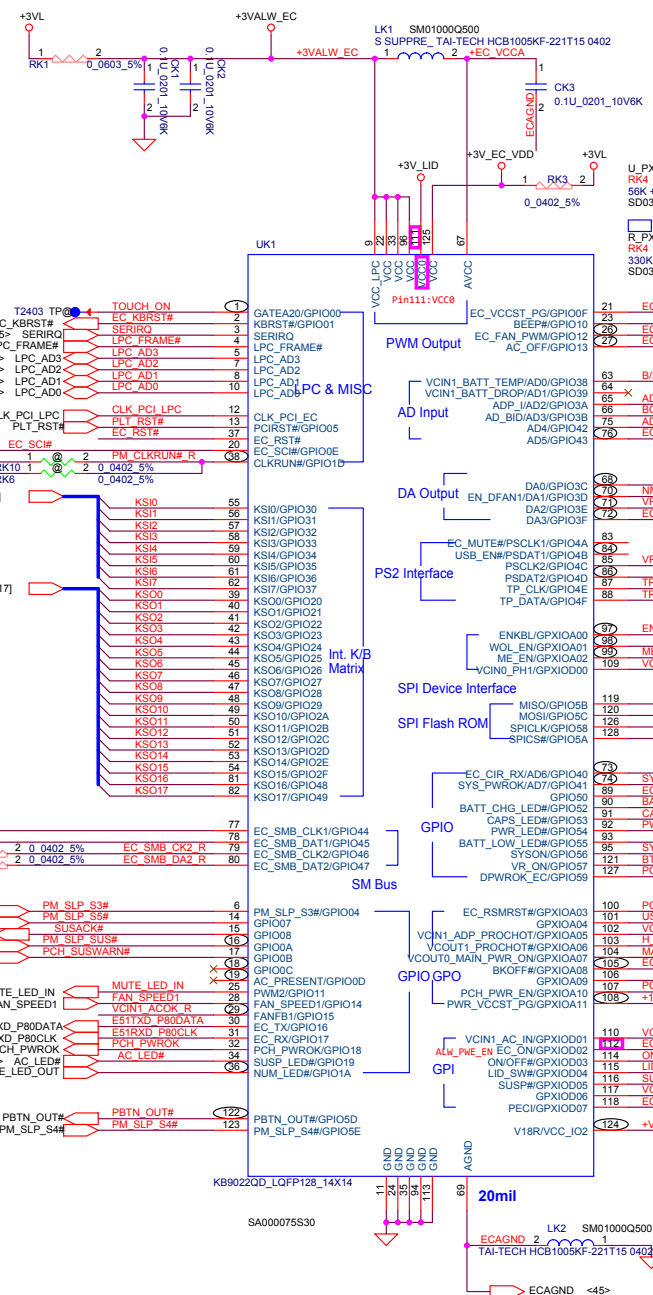
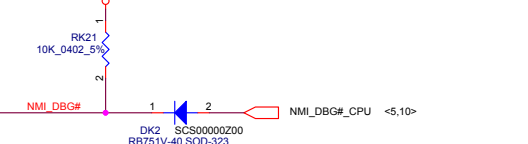
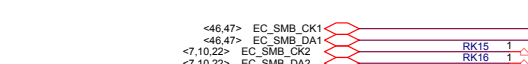
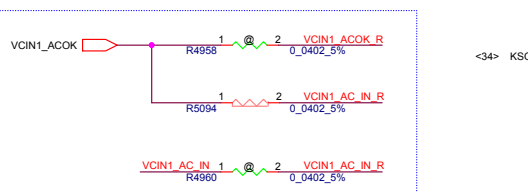
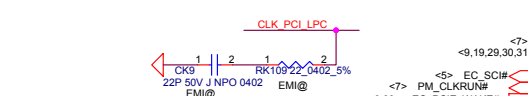
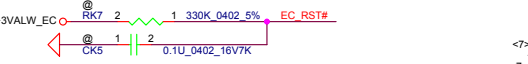
Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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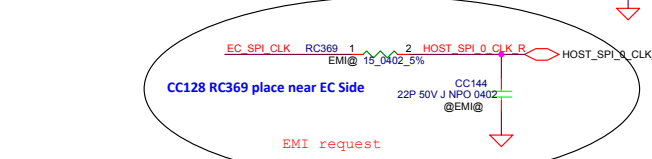
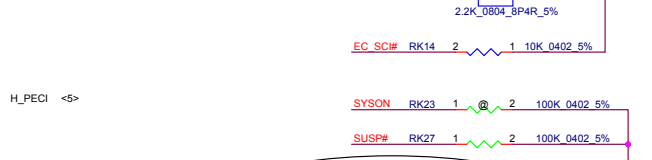
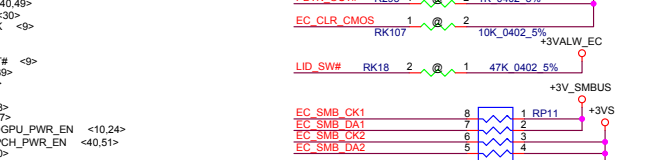
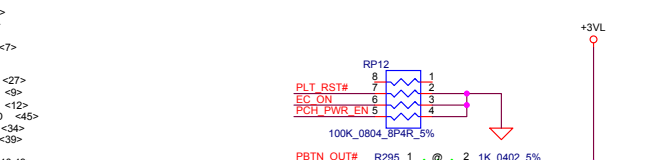
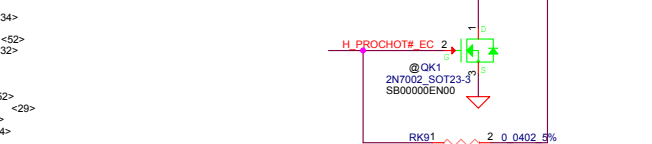
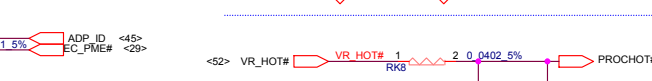
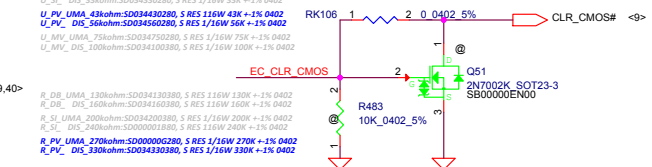
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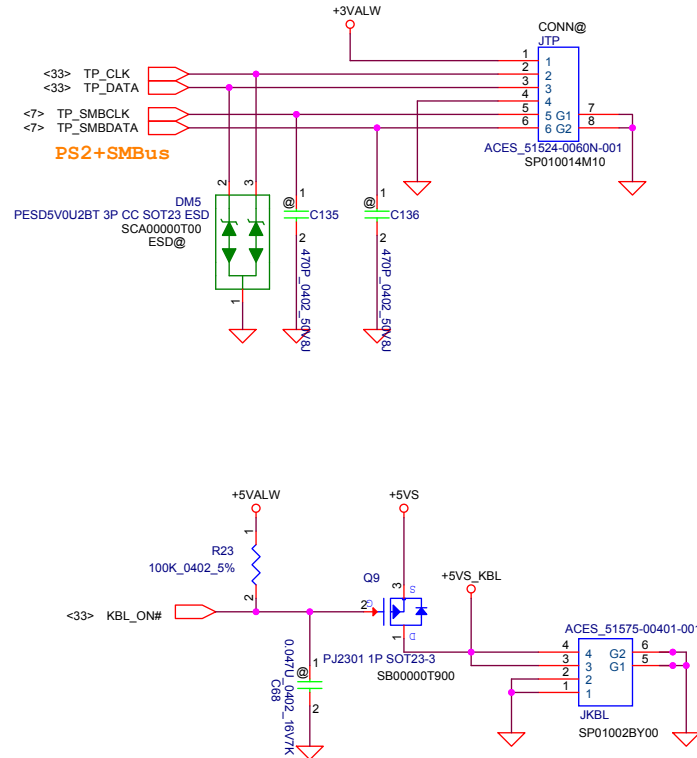
EC Board ID (UMA, DIS, phase) control table

RK4	KBL-U				KBL-R			
	DB	SI	PV	MV	DB	SI	PV	MV
UMA	15K	27K	43K	75K	130K	200K	270K	430K
DIS	20K	33K	56K	100K	160K	240K	330K	560K

Reserve EC_CLR_CMOS for clear CMOS
(2017-03-04: Confirm Intel platform not support EC Clear CMOS function)
(2017-10-05: 201809P add EC Clear CMOS function)

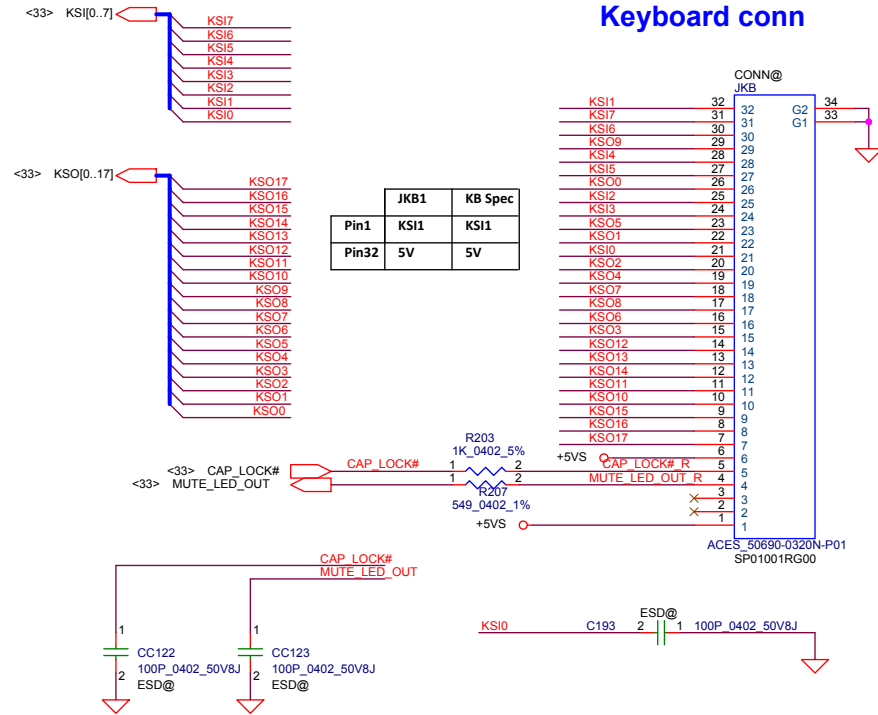


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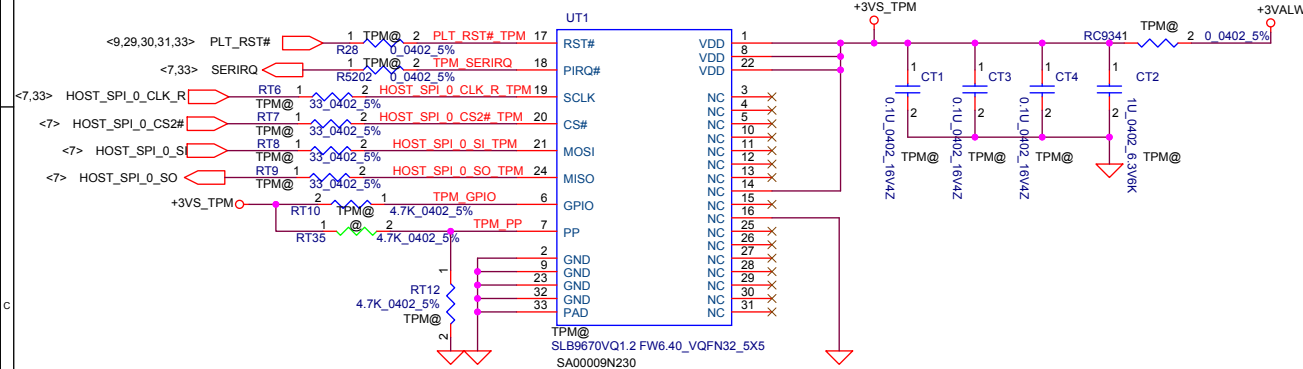


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<12,37,38,39,40,48,49,52,53> +5VALW

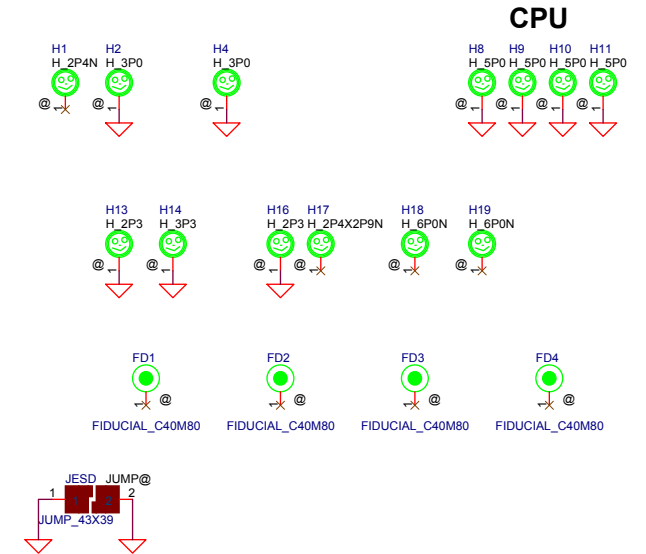
Keyboard conn



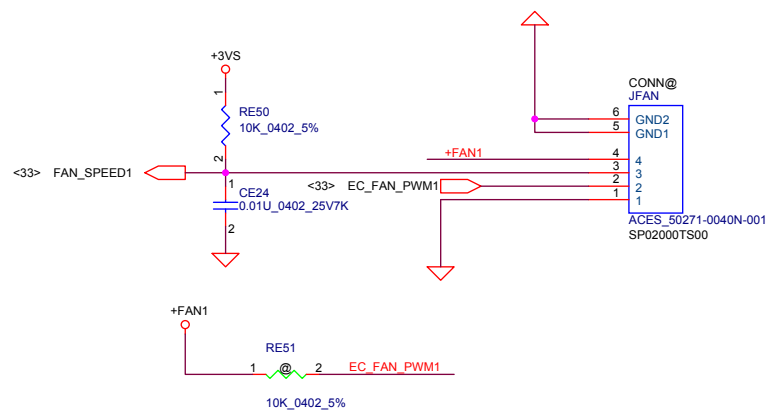
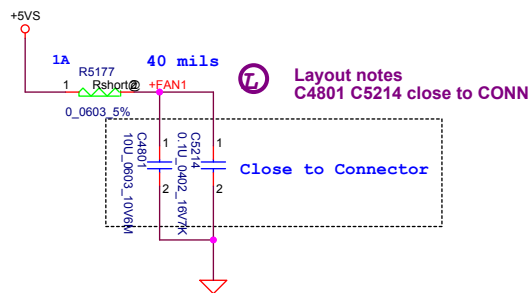
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Screw Hole



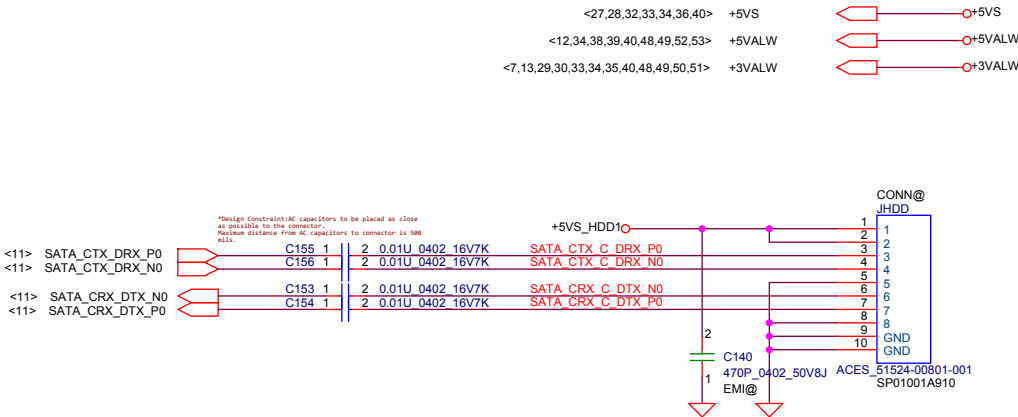
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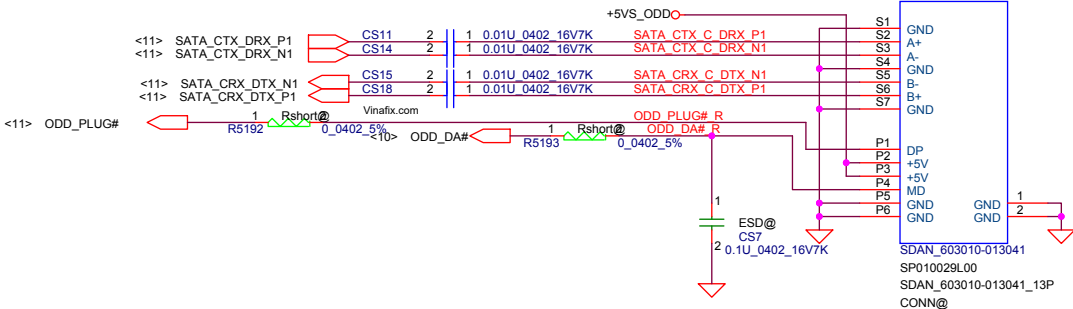
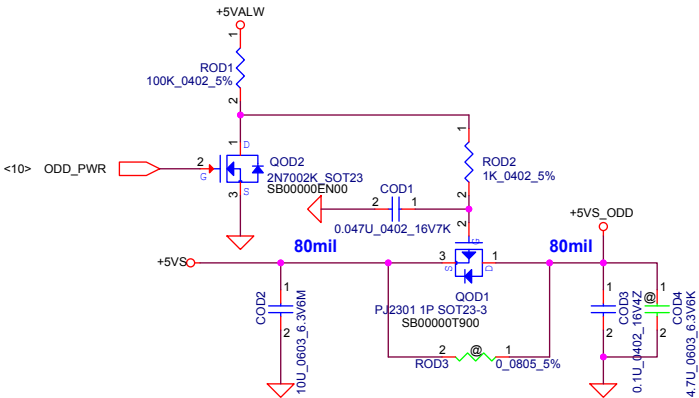
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2.5" SATA HDD

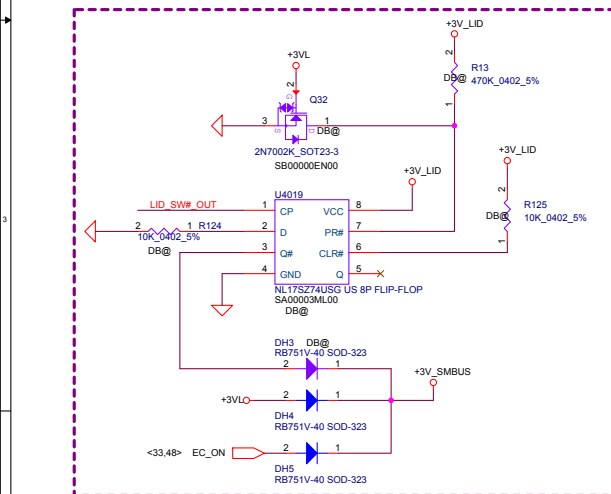
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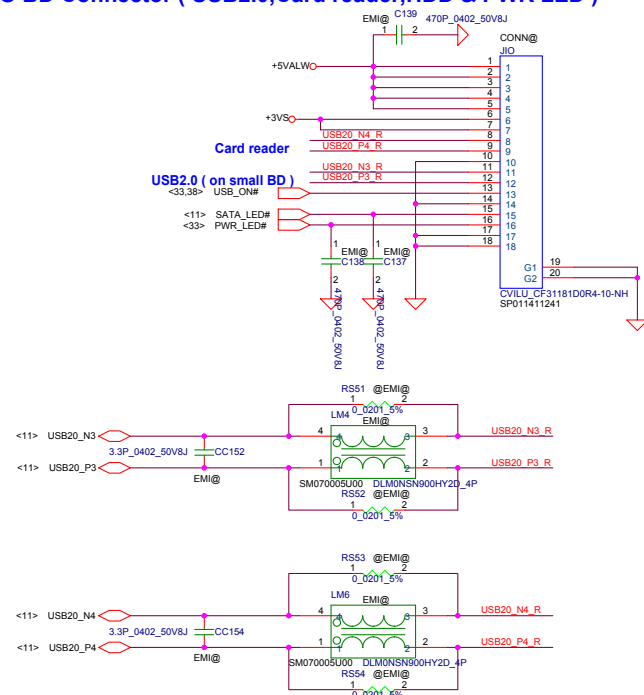
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2017/08/24		2018/08/24		Title	
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IO BD Connector (USB2.0,Card reader,HDD & PWR LED)



5	4	3	2	1
D				D
C				C
B				B
A				A

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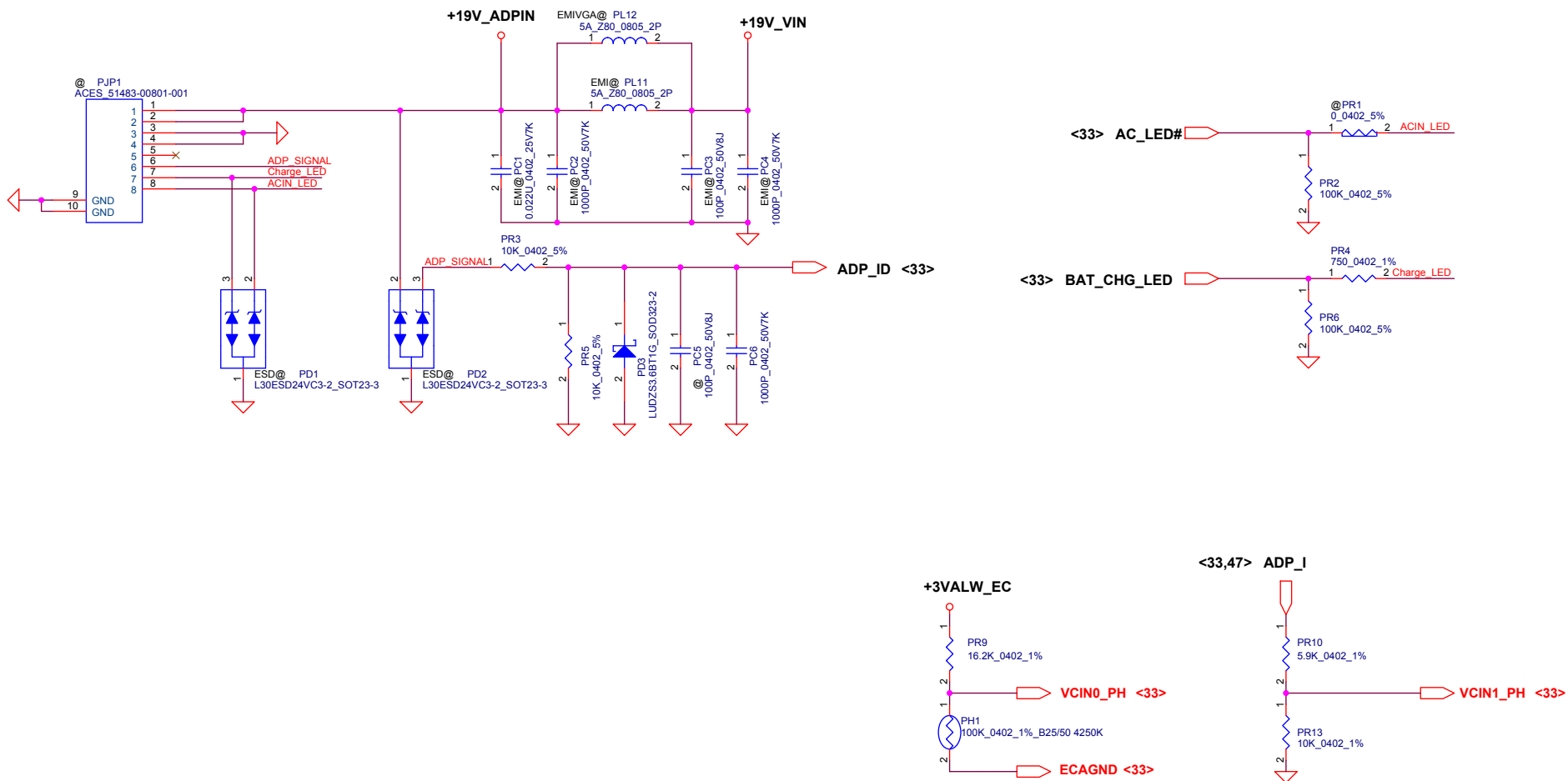
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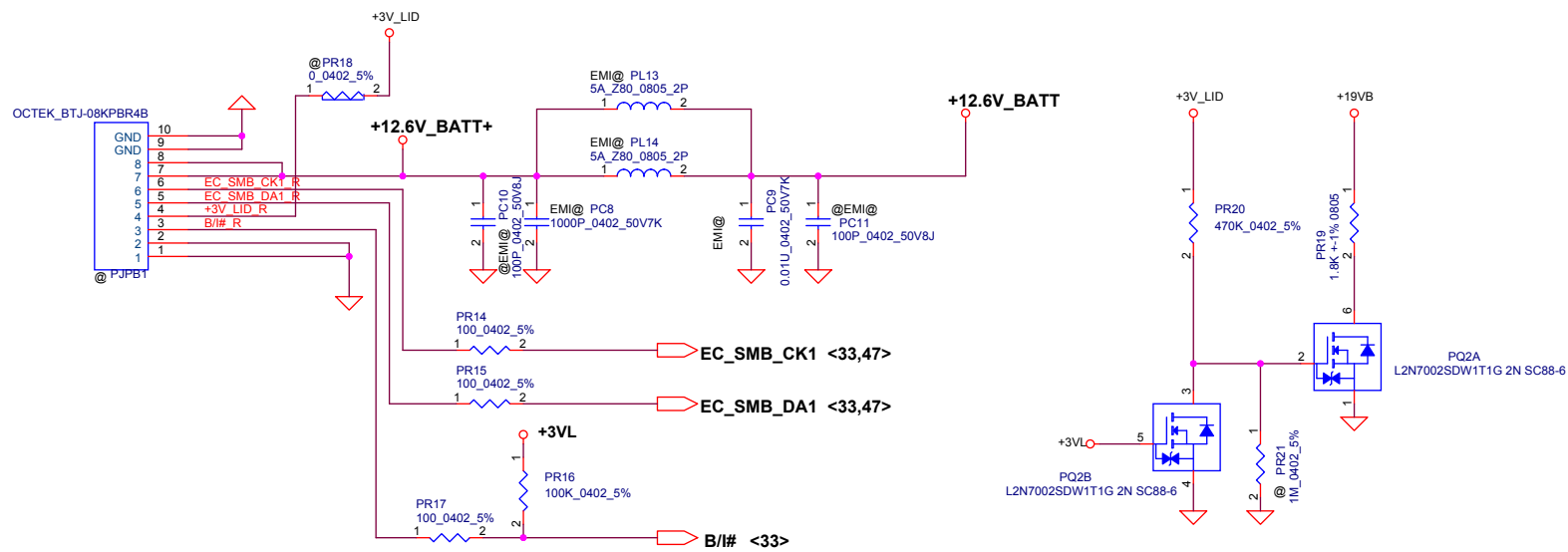
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Date:	Friday, January 05, 2018			Sheet	43	of 59

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C				C
B				B
A				A

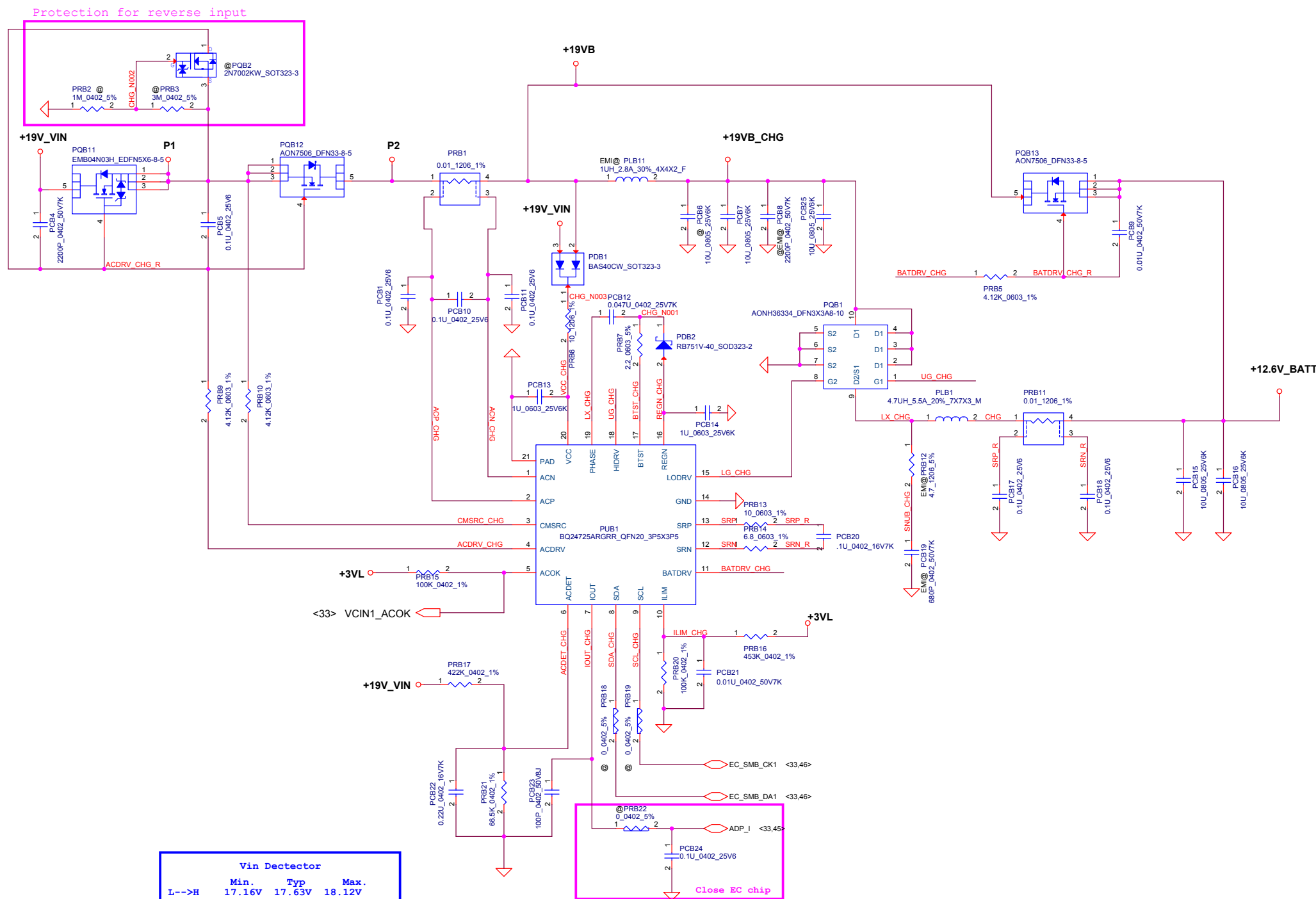
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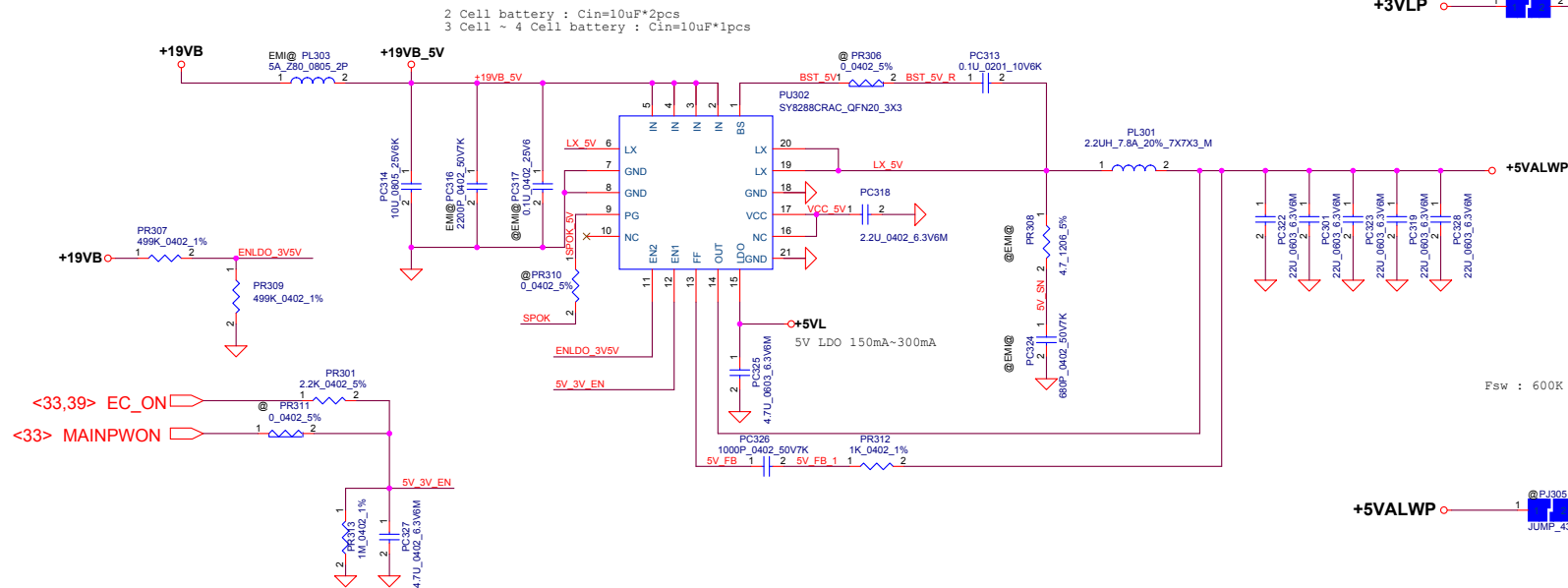
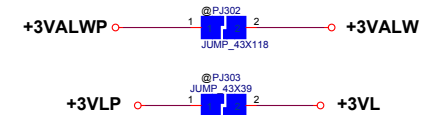
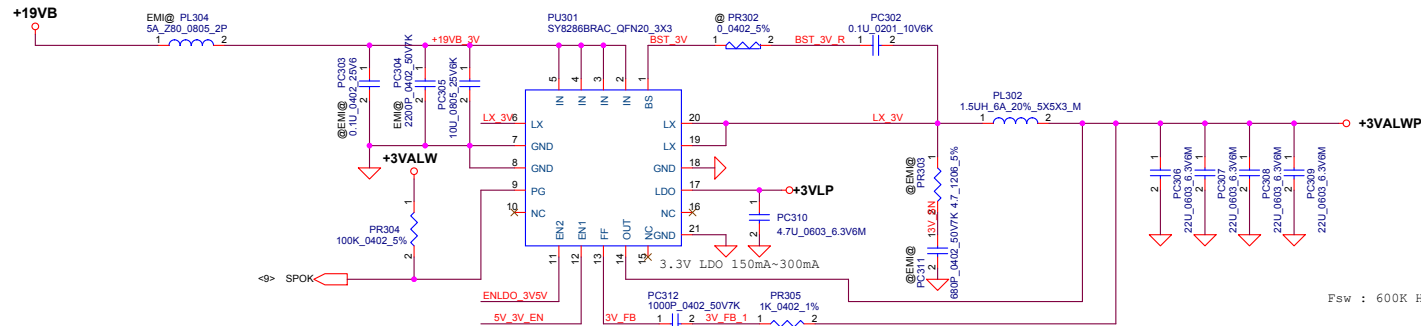


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				Date	Friday, January 05, 2018
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				Rev	v0.3

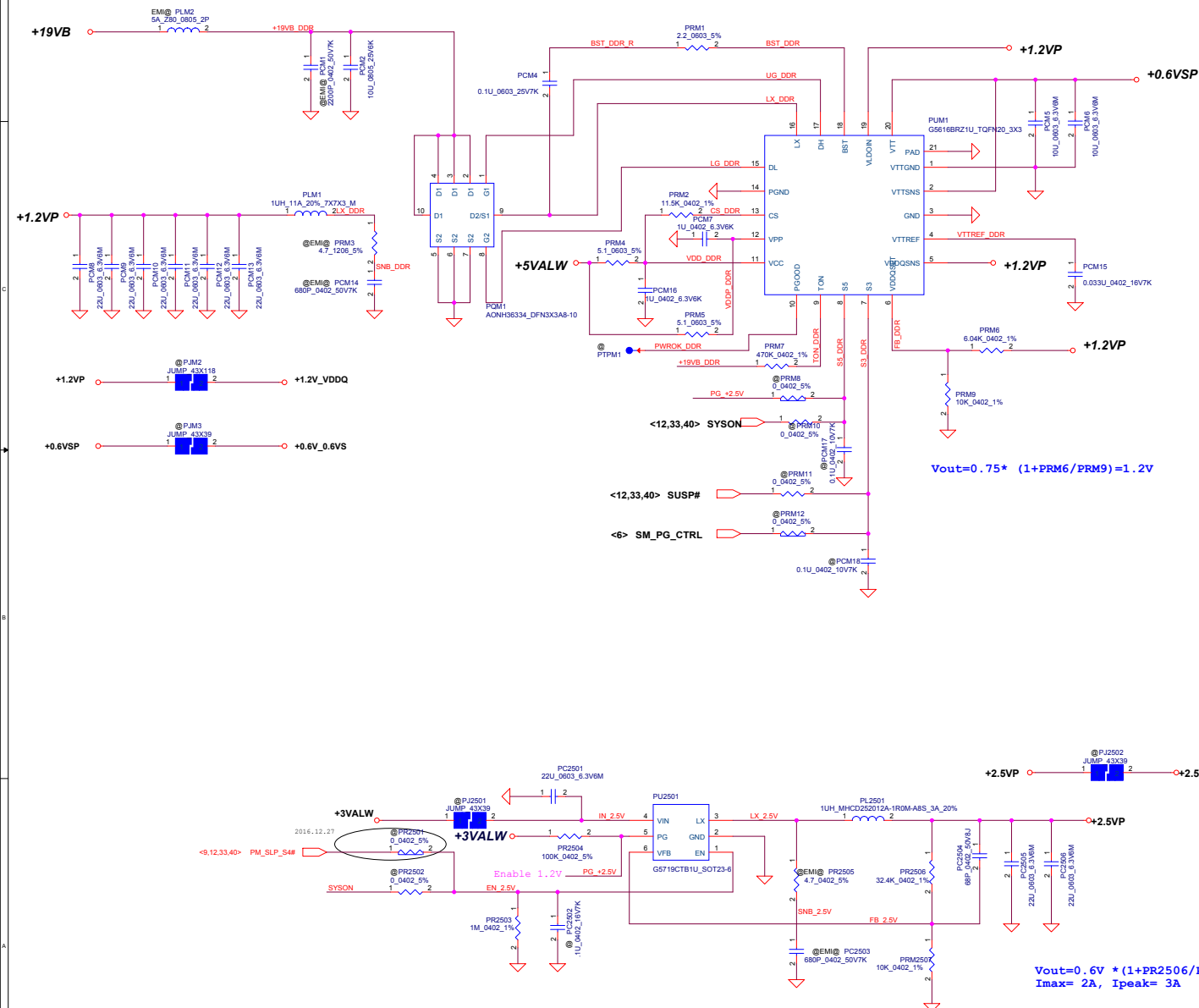



Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

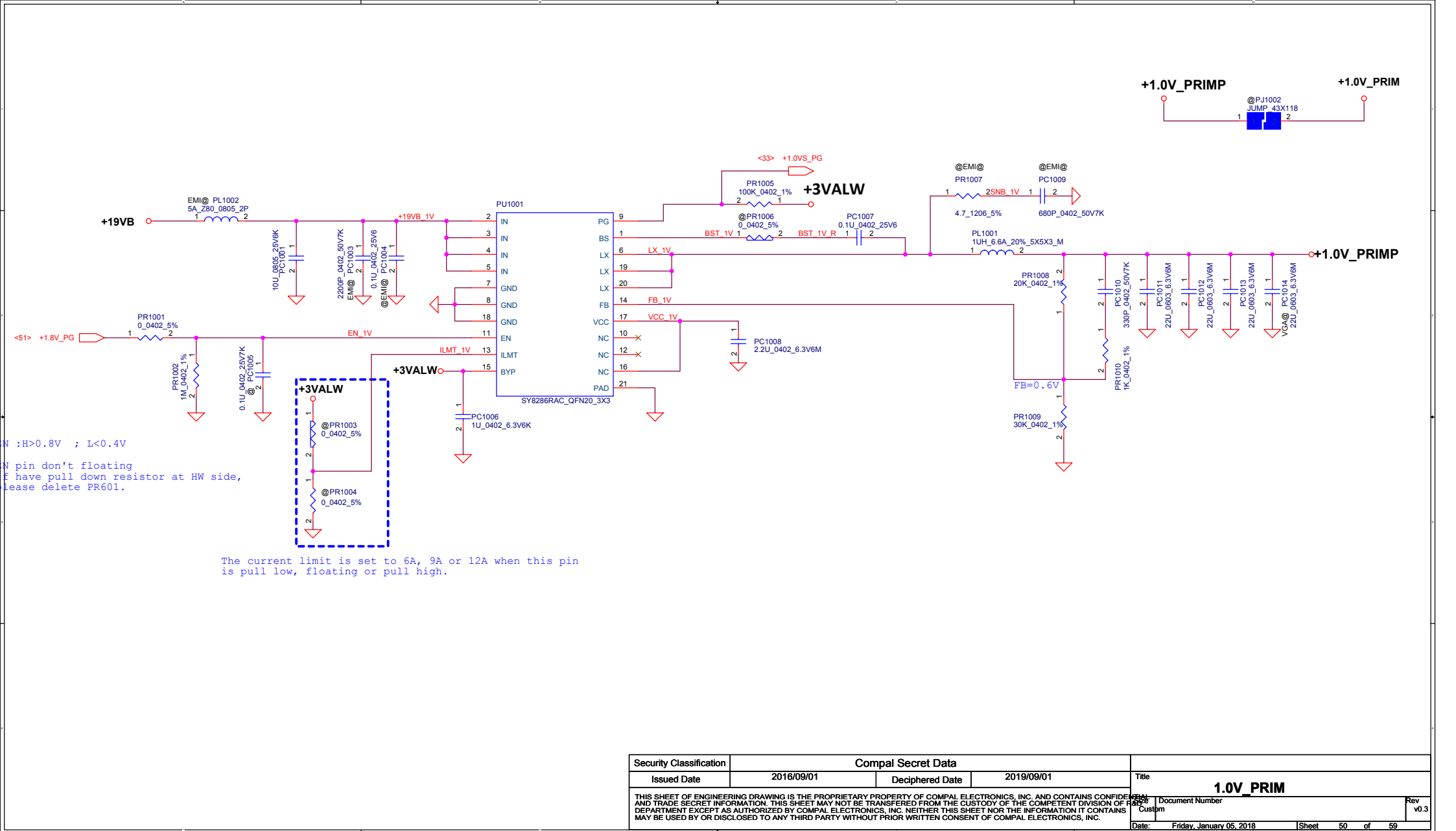
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 $ILIM = 3.3 * 100 / (100 + 620) / 20 / 0.02$
 $= 2.291 A$

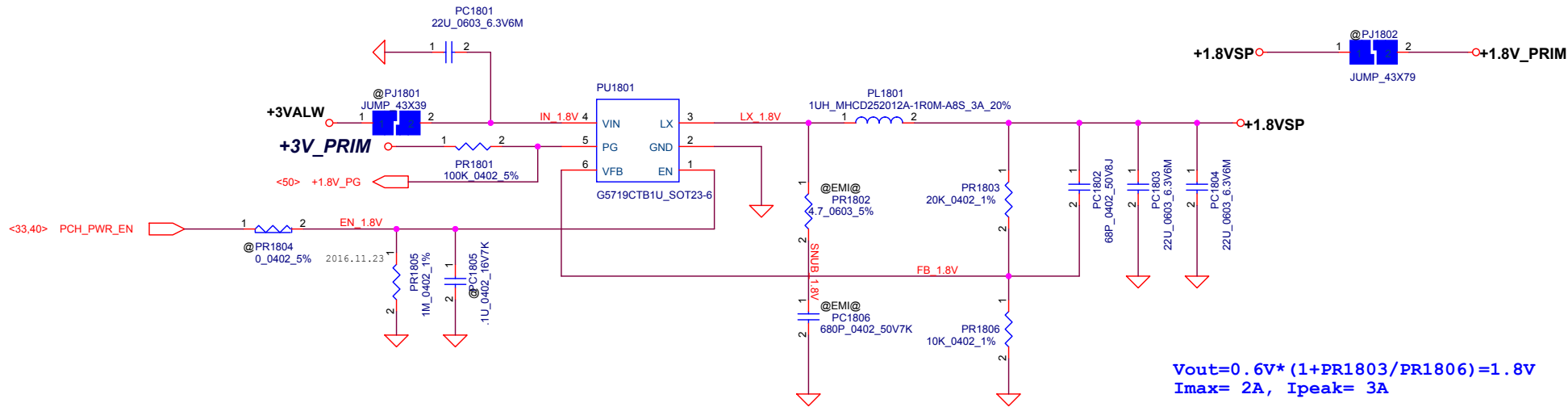


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				v0.3
				Date: Friday, January 05, 2018
				Sheet 46 of 59

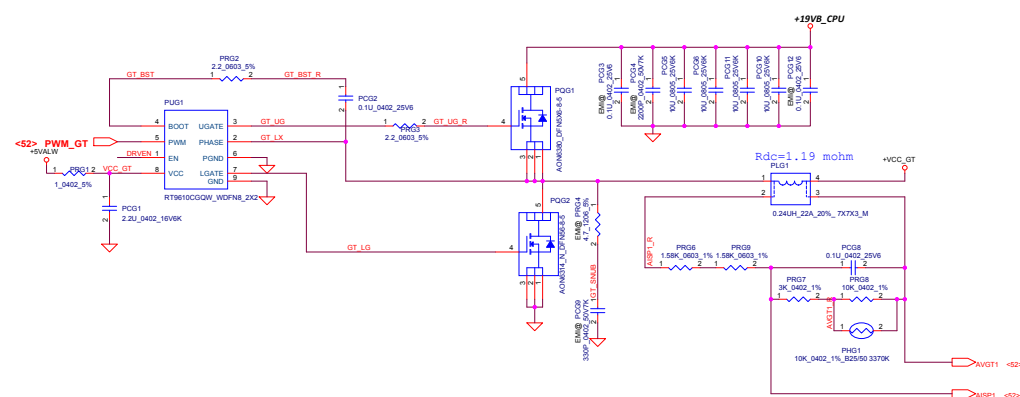
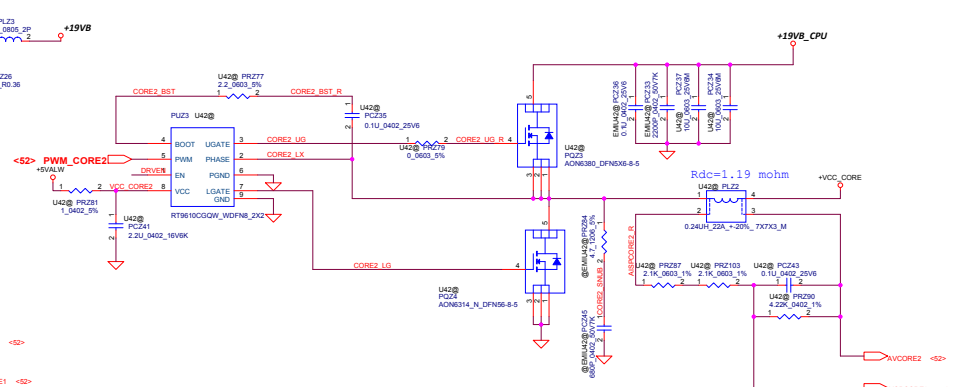


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				Date:	Rev v0.3
				Sheet 51 of 59	



VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

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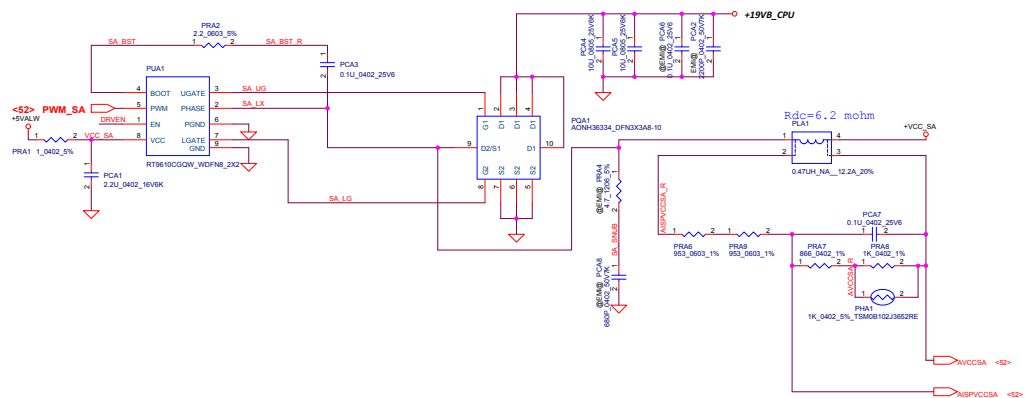
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LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

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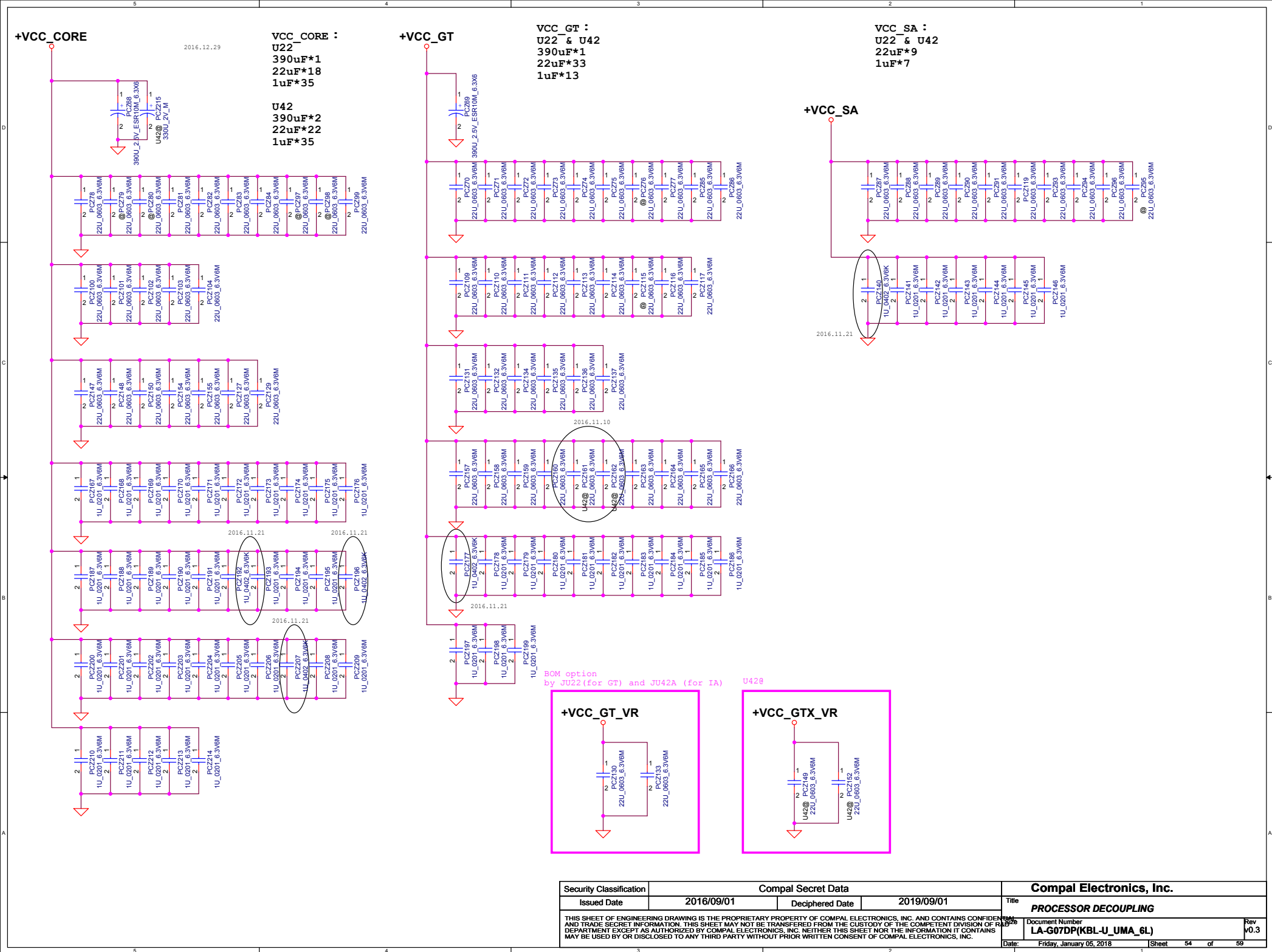
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042
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ICCMAX=5A
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			LA-G07DP(XBL-U, UMA) (BL)	
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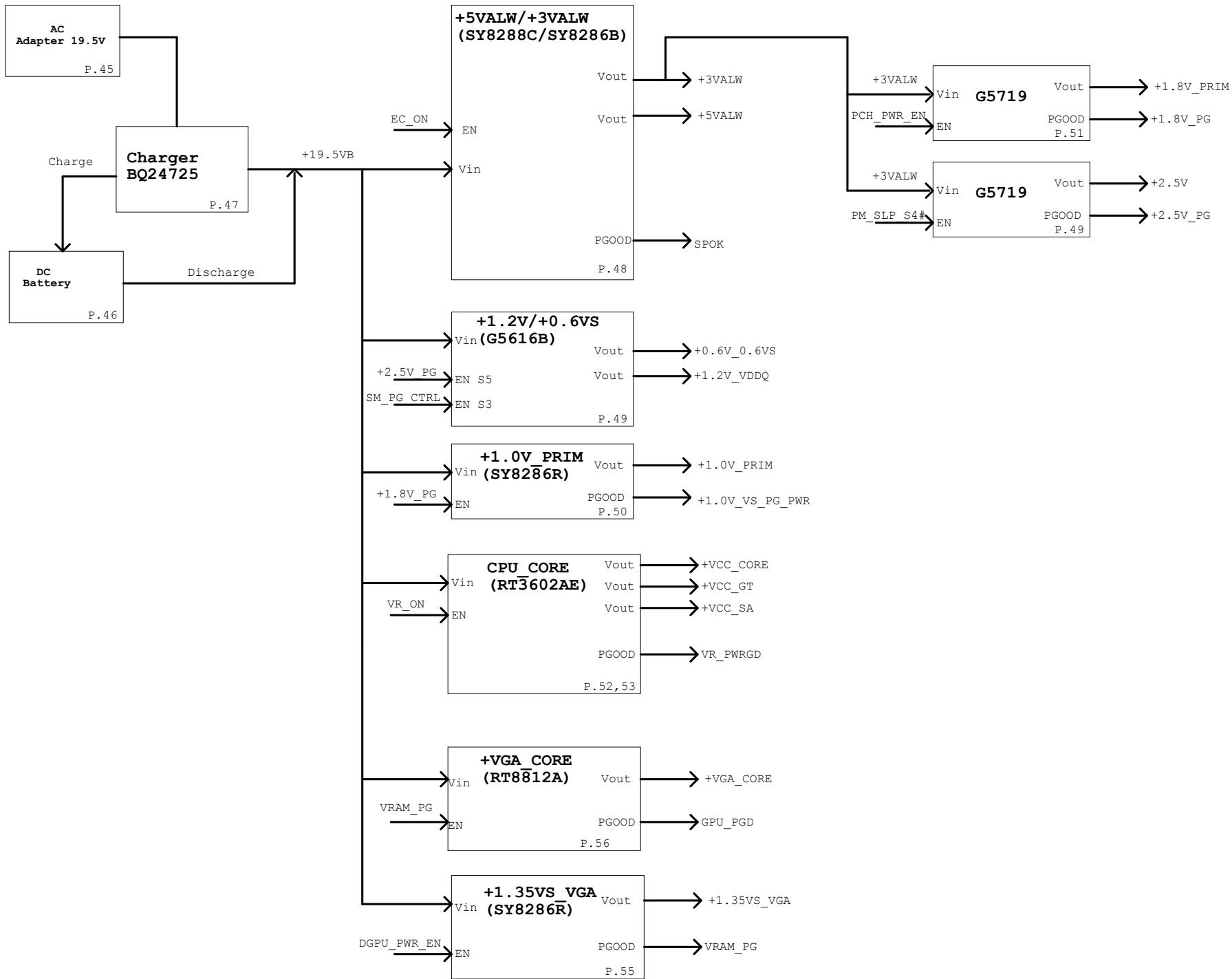


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				Date: Friday, January 05, 2018	Sheet 56 of 59



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				Date:	Friday, January 05, 2018 Sheet 59 of 59